Overview of 3D Architecture Design Opportunities and Techniques

Jishen Zhao
University of California, Santa Cruz
Santa Cruz, CA 95064, USA
jishen.zhao@ucsc.edu

Qiaosha Zou
Huawei Technologies Co. Ltd.
Hangzhou, Zhejiang, China
qszou@cse.psu.edu

Yuan Xie
University of California, Santa Barbara
Santa Barbara, CA 93106, USA
yuanxie@ece.ucsb.edu

***Abstract*—As one of the most promising solutions to the well-known interconnect crisis, three-dimensional (3D) integration attracts plenty of attention from both academia and industry communities. 3D integration techniques enable much shorter interconnect wire length, much higher memory bandwidth, and heterogeneous integration. These benign effects lead to a variety of on-going innovations concerned with modern and future computer architecture design. Yet 3D integration also introduces a few design challenges, including thermal issues, increased fabrication costs, and limited power budget. This paper overviews recent studies on 3D architecture design. We first briefly introduce basics of 3D integration technology and then describe the design challenges and recent innovations of 3D architectures.**[1]

I. Introduction

3D integration may refer to various technologies that share a common salient feature: they integrate two or more dies of active devices in a single circuit. Compared to traditional 2D integration technologies, 3D integration replaces long, global wires (with massive repeaters) with short, vertical or horizontal interconnects. Looking further out, 3D integration introduces a few benign effects that are likely to innovate computer architecture design in a non-traditional manner.

First of all, the reduced interconnect wire length and the declined number of global signals can directly reduce the circuit delay and system power dissipation. A variety of previous studies [1] have demonstrated that the reduced wire length can lead to up to 30% delay reduction in 3D arithmetic unit design. In addition, the reduction in wire length, repeaters, and repeating latches can be translated into power reduction due to the reduced parasitics with the shorter wire length and incorporating previously off-chip signals to be on-chip. For example, Ouyang *et al.* [1] demonstrated 3D-stacked arithmetic units with up to 46% power saving compared with 2D designs.

Second, 3D integration enables high-bandwidth memory due to the wide bus width between the processor and the integrated memory. It releases the constraint of off-chip pin counts, and therefore can dramatically increase memory bandwidth by an order of magnitude. For example, Micron's hybrid memory cube (HMC) [2] can offer up to 160GB/s bandwidth with a 2GB capacity. Today, memory bandwidth is a fundamental performance bottleneck. Modern applications typically adopt large memory working set and increasingly larger number of threads which can simultaneously access the memory. By offering high memory bandwidth, 3D integration can substantially change the way memory hierarchy is designed to support high-performance and energy-efficient data movement.

Third, 3D integration allows different circuit layers to be implemented by different and incompatible process technologies, enabling heterogeneous integration. It enables feasible and cost-effective architecture designs composed of heterogeneous technologies to achieve the "More than More" technology projected by ITRS in future microprocessors. For example, 3D integration allows optical devices to be integrated closely with digital circuits with new architecture designs [3]. 3D integration also allows novel computer architectures to be developed such as hybrid processor cache and memory hierarchy design. Various memory technologies, such as SRAM, spin-transfer torque RAM (STT-RAM), phase-change memory (PCM), and resistive RAM (ReRAM), trade off between performance, power, density, implementation complexity, and cost. A hybrid memory hierarchy incorporated with various memory technologies can be optimized for all metrics [4]. 3D integration is a critical technology that enables such hybrid memory hierarchy designs.

Fourth, 3D integration enables much condensed form factor compared to traditional 2D integration technologies. Due to the addition of a third dimension to conventional 2D layout, it leads to a higher packing density and smaller footprint. This potentially lead to processor designs with lower cost.

As such, both academic and industry communities abound with research studies that examine the rich architectural space enabled by 3D integration, since its debut decades ago. From the academia prospective, comprehensive studies have been performed across all aspects of microprocessor architecture design by employing 3D integration technologies, such as 3D stacked processor core and cache architectures, 3D integrated memory, 3D network-on-chip. Furthermore, a large body of research studied critical issues and opportunities raised by adopting 3D integration technologies, such as thermal issue which is imposed by dense integration of active electronic devices, the cost issues which is incurred by extra process and increased die area, and the opportunity in designing cost-effective microprocessor architectures. From the industry

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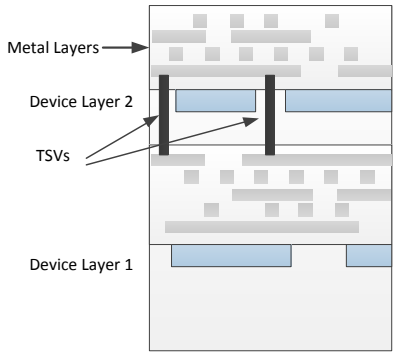
prospective, 3D integrated memory is envisioned to become pervasive in the near future. Intel's Xeon Phi processors will deliver with 3D integrated DRAMs in 2016 [5].

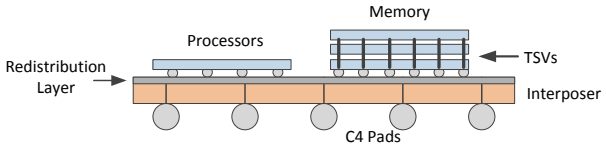
In this paper, we overview recent novel computer architecture designs enabled by 3D integration technologies. We will start from introducing the basis of various 3D integration technologies (Section II). We will then review recent 3D integrated computer architecture designs, including 3D-stacked multi-core processor design, integrated high-bandwidth memory and hybrid memory design, and 3D network-on-chip (NoC) design (Section III). We will also discuss recent studies that investigate thermal and cost issued concerned with 3D integrated architectures (Section IV).

II. 3D Integration Technologies

Based on fabrication processes and medias of vertical interconnects, 3D integration technologies can be roughly categorized as through silicon via (TSV)-based, monolithic, and contactless 3D integration.



(a) TSV-based 3D integration



(b) Interposer-based 3D integration

Fig. 1. A conceptual view of parallel 3D integration.

TSV-based 3D integration (Figure 1(a)) adopts several active device layers which can be fabricated in parallel. These layers are then vertically stacked together to form a single integrated circuit. Typically, TSVs are directly formed in each upper tier before the stacking for vertical interconnect. Therefore, performance of TSVs largely affects the yield of 3D ICs. Steps of 3D fabrication are different from those of 2D counterparts mainly due to the formation of TSVs. In general, four additional steps are necessary for 3D integration, namely etching, thinning, alignment, and bonding [6]. In terms of the bonding orientation, we can classify the bonding into face-to-back (F2B) and face-to-face (F2F) bonding methods. F2F bonding enables higher interconnect density via Cu-Cu bonding on the top metal layer and results in no silicon area overhead for inter-layer signals. I/O signals connecting to the package In contrast, due to the alignment precision and the interconnect size, the interconnect density in F2B is relatively smaller. Three different stacking strategies can be achieved: wafer-to-wafer (W2W), die-to-wafer (D2W), and die-to-die (D2D) stacking. The major difference among these three is whether to slice the wafer into dice before stacking. For W2W stacking, wafers are bonded before sliced into dice. This process has the highest productivity yet the lowest compound yield. Testings are required for D2W and D2D stacking and only known-good dies (KGDs) are selected for bonding. Therefore, the compound yield is increased by preventing bad dies from stacking on good ones.

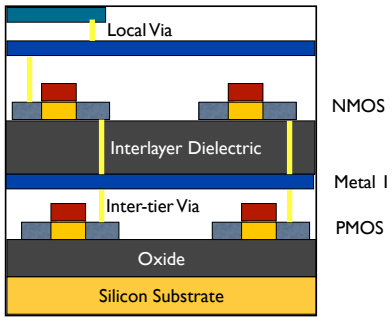


Fig. 2. A conceptual sketch of sequential/monolithic 3D integration.

To reduce the manufacturing complexity and fabrication cost, recent 3D IC designs employ an alternative integration technique, interposer-based integration techniques, which is also known as 2.5D integrated circuits (Figure 1(b)). Interposer is a connection media containing only interconnect components (TSVs, BEOL, etc.). With 2.5D integration, dies incorporated with active devices are integrated horizontally on the silicon interpose and connected by signals going through TSVs.

Monolithic 3D integration [7] (Figure 2) successively grow device layers on a conventional CMOS or silicon-on-insulator (SOI) plane. Devices on the bottom layer are fabricated with traditional fabrication processes. The fabrication technique for upper layers is challenging because of two extra requirements: first, we need to guarantee device electrical characteristics in the upper layers after fabrication, such as field mobility and threshold voltage; second, building upper planes cannot compromise the electrical performance of the bottom layer. By employing sequential fabrication process, monolithic 3D ICs allow the pitch of vertical interconnects smaller than TSVs. Therefore, monolithic 3D integration technology enables finer-grained stacking at gate level or even transistor level.

Contactless 3D integration employs coupling of electric or magnetic fields to perform the interlayer communication with a comparable data rate as TSVs. Based on the coupling principle, contactless 3D integration can be further categorized into capacitively and inductively coupled 3D integration [8]. The major benefit of contactless 3D integration is that the

fabrication process is compatible with 2D processes. However, the inductors and capacitors can dissipate certain amount of power. For example, although the inductive-coupling can consume only 0.14pJ per bit, the energy consumption of the inductors is continuous, wasting significant amount of power [9], [10].

Comparison of 3D integration technologies: Compared to TSV-based 3D integration, monolithic integration can lead to up to 8% smaller area due to smaller size of inter-tier via than the TSVs, 12% lower longest path delay, and 7% lower power [7]. Nevertheless, implementing monolithic 3D ICs requires non-trivial changes to conventional fabrication process, making it less practical compared to the TSV-based approach. One of major issues with contactless transmissions is the significant metal area consumption introduced by coils and metal plates, especially when high transmission intensity is required in inductively coupled designs. For example, the coil diameter is $60\mu m$ for one signal in a $25\mu m$ communication distance [8]. Due to the design infeasibility, fabrication complexity, and cost issues, monolithic and contactless 3D integration is less commonly found in existing 3D architecture designs. Most previous designs employ TSV-based 3D integration technology.

III. 3D Architecture Design

3D integration introduces a third dimension to circuit design, opening doors to numerous of novel computer architecture solutions towards high-performance, cost-effective, and energy-efficient computer designs. For decades, computer architects have invested substantial effort in exploring this new design space enabled by the emerging 3D integration technologies. In this section, we review a few representative works among these research efforts.

A. 3D-stacked Multi-core Processors

3D integration technologies offers computer architects with opportunities in designing novel multi-core processor architectures, with various processor function units being separated and stacked in multiple layers [11]. Compared to traditional 2D designs, such 3D-stacked multi-core processors promise shorter interconnect delay between function units, smaller form factor, and reduced interconnect power dissipation. For example, Zhao *et al.* [11] explored the design space of 3D many-core processors by partitioning processor cores and caches in two different manners: homogeneous partitioning tiles each processor core and L2 cache bank together and each layer incorporates several such tiles; heterogeneous partitioning places processor cores and the L2 cache in different layers. Their study investigated the fabrication cost and thermal effect of the two design strategies. Recent studies also explored the optimal 3D-stacked processor caches.

B. High-bandwidth Memories

The prominent "memory wall" problem limits the further performance improvement of multi-core processors. 3D stacked memory with computing logic in one die has been envisioned as one of the early commercial adoption of 3D integration. In addition to offering high memory bandwidth, such 3D integration also eliminates the redesign complexity which is required by fine-grained partitioning involved with 3D-integrated processor designs. The 3D stacked memory can be implemented with two typical approaches: TSV-based 3D stacking and interposer-based 2.5D integration. With 3D stacked memory, building memory layers directly on top of logic layers requires close collaboration between microprocessor vendors and memory vendors. Complexity of thermal management can pose challenges on the heat sink design, layer allocation, and floorplanning. In contrast, employing interposer-based 2.5D integration can alleviate such design burden and decouple the memory design from more complex processor designs. Such design strategy has been demonstrated by Micron's Hybrid Memory Cube (HMC) [2] and JEDEC High-bandwidth Memory (HBM) standard [12]. HMC [2] combines high-speed logic process technology with a stack of TSV bonded memory die. It offers as much as 400GB/s bandwidth, while consumes 70% less energy per bit compared with state-of-the-art DRAM technologies. HBM [12] initially targets at graphic applications. Recently, AMD and SK Hynix announced joint development of HBM stacks, which leverages TSV and wide I/O technology and conforms JEDEC HBM standardization.

Besides traditional DRAM based memories, 3D integration provides another promising design opportunity in integrating the emerging nonvolatile memory (NVM) with conventional processor and memory architectures. Most NVM technologies are incompatible with the CMOS technology. They can introduce additional process steps besides the traditional CMOS process. Implementing a computer system with NVM can incur substantially increased fabrication cost. 3D integration allows heterogeneous technologies to be integrated in a single circuit. Consequently, it eases the adoption of NVMs in CMOS-based microprocessors. With separate fabrication process, NVMs and computing logics can be optimized accordingly to enable high flexibility, cost-effective, and high performance architecture [13].

C. 3D/2.5D Integrated DRAMs as Cache and Memory

With 3D integration, it is possible to integrate a large-capacity DRAM (several gigabytes) with the processor. Several recent studies explored the design space of employing the integrated DRAM either as the last-level cache (LLC) [14] or part of the main memory [15]. The two design options trade off performance, storage overhead, and design complexity; no one-size-fits-all solution exists. As such, a natural extension is to dynamically switching the integrated DRAM between the roles of LLC and main memory. Chou *et al.* [16] proposed an on-chip memory design, which is managed as a LLC yet exposed to the OS as a portion of the physical address space. To this end, their design exposes the 3D-stacked DRAM to the OS, but manages it at the cache line granularity. When a miss happens at the stacked DRAM, the design swaps the data fetched from the off-chip main memory with an

existing memory line in the stacked DRAM. In this manner, the proposed design sustains the latency and the bandwidth benefits of the stacked DRAM.

D. 3D/2.5D GPUs

Graphics processing units (GPUs) require extensive memory bandwidth to support the data access of massively parallel executing threads. With the benefit of providing high memory bandwidth, 3D integrated memory is a promising candidate for graphics memory. This promising design opportunity has been explored by a couple of recent studies on energy-efficient GPU design with reconfigurable in-package graphics memory [17], [18]. Shortly after the academic studies were published, two top GPU vendors are both considering to introduce 3D integrated graphics memory into their future products. NVIDIA announced that 3D integrated memory will be adopted in their new GPU products in 2016 [19]. AMD plans to ship high-bandwidth memory (HBM) with their GPU products and heterogeneous system architecture (HSA)-based CPUs in 2015 [20].

E. 3D NoCs

With more and more cores are integrated in a single system, the inter-core connection with buses cannot fulfill communication requirements between cores. Network-on-chip (NoC) is therefore emerging to tackle the communication scalability problem. In this subsection, we consider moving NoC above cores instead of designs of router and routing algorithm to adapt the vertical connections.

3D Interconnect Service Layer (ISL): In 2D designs, NoC designs are constraint by the limited routing resource and silicon area. This limitation can be relaxed with 3D integration by building a single layer for interconnects, which decouples the interconnect component from computing and storage units. This separated interconnect layer is defined as Interconnect Service Layer (ISL) by Wu *et al.* [21]. The benefits of building separate layers for NoCs are as follows: the manufacture cost can be reduced due to the smaller die area after moving NoCs from computing layers; more reliable and flexible interconnect designs can be applied without the silicon area limitation; multiple network topologies can be supported in a single chip for different connection requirements. In their work, the core performance of using a hybrid mesh topology with coarse-grained and fine-grained meshes is improved compared to the baseline 2D design.

3D optical NoC: Optical NoCs are emerging to meet the continuously increased communication bandwidth problem. However, fabricating optical components on the core layer increases fabrication cost and the performance of optical components might be affected by the high core temperature. Therefore, the 3D integration enables the heterogeneous integration of optical dies and CMOS processor dies. For example, the Corona architecture proposed by HP Labs leverages the 3D stacking to build a nanophotonic NoC in multi-core system for both inter-core and off-chip communications [3]. Even though the optical NoC provides low power and high bandwidth, it faces the challenges of the thermal sensitivity and process variations, which may result in performance degradation or even malfunction if they are not properly addressed.

IV. 3D Architecture Challenges

Due to technology limitations and the absence of mature design methodologies, designing 3D architectures can be a challenging task. Among these challenges, we describe the two most critical ones in this section.

A. Design and Fabrication Cost

One major concern about adopting 3D architectures is the cost of design and fabricating such chips: Will 3D integrated processors and memories incur higher cost than their 2D counterparts? A couple of recent studies comprehensively analyzed the cost issue and show that 3D integrated architectures can in fact cost less than 2D designs by adopting proper design strategies.

In correspondence to the fabrication process, the 3D cost can be divided into five parts: wafer cost, bonding cost, testing cost, package cost, and cooling cost. The wafer cost captures the silicon and device formation cost of each separate die. Different from 2D designs, the introduction of TSVs results in area overhead, which in turns affect both the silicon area and die yield. The bonding cost estimates the cost during TSV forming, wafer thinning, and bonding. The TSV forming cost varies with different TSV fabrication processes and stages. In several recent studies [11], [22], the etching and TSV last approach are used, because the separation between die fabrication and TSV forming enables the decoupling between wafer cost and bonding cost. The extra testing cost in 3D ICs can be captured in the model proposed by Chen *et al.* [23]. The study shows that D2W integration has higher testing cost. However, when combining with the fabrication cost, it is still more favorable because of the high stacking yield.

The package cost is determined by the package type, the package area, and the pin count. From their study [11], [22], the pin count is identified as the dominant factor in 3D integration. In addition, the cooling cost is expected to be higher in 3D integration because the increasing on-chip temperature needs more powerful cooling solution.

These additional costs from 3D integration make the 3D enabling point critical for making the design decision. 3D integration is cost efficient only when the cost saving from reduced silicon area outweighs the bonding, testing, and cooling cost. In Dong's study [22], they find that 3D designs are cost efficient only when the design exceeds 50 million gates per chip with $65nm$ technology node. With advanced processing technology, the enabling point moves towards larger number of gates. Moreover, when the number of gates per chip increases, stacking more layers is considered to have cost saving.

The cost issue in 3D ICs attracts plenty research efforts in performing test cost optimization, yield enhancement, and TSV reduction [24].

B. Thermal Issues

Thermal is another challenging issue in 3D architecture design due to two aspects. The first reason lies in the increasing power density of 3D stacking. Small form factor and large number of stacking layers deteriorate the thermal dissipation. The second reason is the lack of sufficient thermal dissipation path from devices to the ambient or the heat sink, leading to the elevated on-chip temperature. The high on-chip temperature causes many performance and reliability issues, such as thermal runaway and accelerated electromigration. Therefore, it is significantly important to perform 3D thermal modeling/analyses and deploy efficient thermal management schemes.

Thermal modeling. Two 3D thermal models are commonly used in thermal analyses. The first model is using partial differential equation to represent the on chip temperature from Sapatnekar *et al.* [25]. Equation 1 can be used to calculate the transient thermal response with Poisson's equation as steady state and additional boundary conditions. Two methods can be applied to solve this equation: the finite difference method (FDM) and the finite element method (FEM).

$$\rho c_p \frac{\partial T(r,t)}{\partial t} = k_t \bigtriangledown^2 T(r,t) + g(r,t) \tag{1}$$

The FDM and FEM computation overhead is large, which is inappropriate for thermal analysis in design space exploration. Therefore, the second compact thermal model is proposed as building the equivalent thermal circuit. This model is widely used in thermal analyses. The devices are viewed as thermal resistance and capacitance. The value of resistivity represents the capability of thermal dissipation. The higher the value is, the harder the thermal dissipation can be. Heat flows are modeled as currents while the temperature differences are modeled as voltages. The thermal capacitance captures the delay before the temperature reaching the steady state. The dominant factor to determine the circuit temperature is the heat conduction to the thermal package and to nearby circuits.

Thermal management schemes. Generally, thermal management can be performed in either design time or run time. In design time, methodologies on thermal-aware physical level design (floorplanning, place and route, and power planning) have been extensively explored [26]. Thermal via insertion is another attractive solution [27]. Dummy vias are inserted above hot spots to help vertical thermal dissipation by leveraging the high thermal conductivity of conductive materials. In addition to above mentioned methods, powerful liquid cooling methods are attractive for 3D designs [28]. During run time, numerous 2D thermal management schemes can be applied on 3D designs, such as dynamic voltage and frequency scaling (DVFS) and power gated.

Thermal-aware architecture design. 3D processors can employ thermal herding techniques [29] to herd or steer the switching activity to the die that is closest to the heat sink and reduce the total power (and power density). Thermal herding is proposed based on the observation that only a few of the least significant bits are needed in the data used in many integer instructions. Therefore, the datapath can be organized by assigning each 16 bits to a separate dies (4 dies) in 3D stacking; we can place the least significant bits on the top layer which is closest to the heat sink. Beyond addressing thermal issues, 3D thermal herding techniques can also improve system performance by reducing the pipeline depth and L2 cache latency; power is also reduced due to the reduced wire length and switching activities (because of clock gating). The thermal experiments show that thermal herding techniques successfully control power density and mitigate 3D thermal issues.

C. Testing Challenges

Compared to traditional 2D IC fabrication, 3D IC fabrication incorporates more intermediate steps, such as die stacking and TSV bonding. Because of these extra steps, 3D IC manufacturing typically performs wafer test before final assembly and packaging. Wafer test for 3D ICs has challenges: First, existing probe technology cannot perform finer pitch and dimensions of TSV tips, hence is limited to handling only several hundred probes at a much lower number than required TSV probes; Second, wafer test can require to create a known-good die (KGD) stack, which can risk damaging due to the contact of the highly thinned wafer by a wafer probe; Third, 3D ICs can also impose intra-die defects caused by thermal issues and new manufacturing steps, such as wafer thinning and bonding the top of a TSV to another wafer. Recently, Wang *et al.* [30] proposed a built-in self test methodology to test TSVs in 3D ICs prior to stacking. They also developed efficient architecture and circuit design to perform the pre-bond TSV scan testing. While 3D IC testing is a crutial problem, testing aware 3D architecture design has remained largely unexplored in the research community and require substantial efforts in addressing the testing challenges.

D. 3D Placement Challenges

Based on the block position decided by floorplanning, the cell/gate position is determined during placement. Different from 2D designs, the 3D placement not only needs to consider the cell spreading on the xy plane, but also in the vertical direction. If temperature is the primary concern, then cell placements on the upper layers should be sparser than the bottom layer which is near heat sink. Temperature and wirelength are two major design objectives during placement. Various placement methodologies are presented by previous studies. For example, Athikulwongse et al. [26] proposed two thermal-aware global placement algorithms employing the force-directed methodology to exploit the die-to-die thermal coupling in 3D ICs. The first algorithm generates forces for TSV spreading and alignment for better heat dissipation path. The second algorithm builds forces based on thermal conductivity in cells and on power density for TSVs. Their second methods can achieve the best temperature results among state-of-the-art placers.

V. CONCLUSION

3D integration is one of the most promising solutions for future computing system. In this survey paper, we review

recent innovations in 3D architecture design. Furthermore, we also analyzed the two major challenges in 3D integrated processor and memory designs, including cost and thermal issues. Although the community has gained initial success on 3D integration, yet substantial work are needed to further improvements on 3D architecture designs and the exploration of killer applications are still needed.

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