CPDI: Cross Power Domain Interface Circuit Design in Monolithic 3D Technology

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Abstract — Optimizing energy consumption for electronic systems has been an important design focus. Multi-power domain design is widely used for low power and high performance applications. Data transfer between power domains needs a cross power domain interface (CPDI). The existing level-conversion flip-flop (LCFF) structures all need dual power rails, which leads to large area and performance overhead. In this paper, we proposed a CPDI circuit utilizing monolithic 3D technology. This interface functions as a flip-flop and provides reliable data conversion from one power domain to another. Our design separates power rails in each tier, substantially reduced physical design complexity and area penalty. The design is implemented in a 45nm low power technology. It shows 20%-35% smaller clock to Q and 30% energy saving comparing with existing LCFF designs. The proposed design also shows better robustness with ±10% voltage variation.

Keywords — Multi-Power Domain, Level Shifter, Monolithic 3D, Flip-Flop

I. Introduction

Reducing power consumption has become a first-order design goal in today’s high performance and mobile applications. In mobile space, a nearly doubled annual growth of data demand and a mere 6-8% annual improvement of battery capacity quickly deplete the available battery charges. In the meantime, as technology continues scaling, more and more transistors are packed into a smaller area, local hot spots and heat dissipation also impose tremendous challenges to high performance logic systems, leading to the “dark silicon” dilemma [1]. In the past, power consumption problem was tackled at architecture and system levels. More recently, however, low power device technologies also draw considerable attentions [2] and a device-IC design co-optimization is making its way to IC design community [3].

In SoC design, a common solution is to divide the system into different power domains. For example, at coarse level, computational logics and cache can be designed to operate at their own supply voltages. In multi-core system, multi-power-domains is required to facilitate dynamic voltage and frequency scaling for each core (DVFS) [4] [5]. Generally, finer granularity of power domains is known to reduce system power more effectively and is considered as an attractive approach of mitigating the power wall problem. [6]

Multi-power-domain design requires logic level shifter at the domain boundary to assure reliable cross domain data transfer and manage cross domain data traffic. Several level shifters were published in the past [7] [8] [9]. These level shifters are, however, area and performance inefficient, when connecting with flip-flop. Recently, sequential logic cell integrating level shifter function has been proposed in master-slave flip-flop design [10] [11]. The designs were shown to minimize area penalty and reduce cell delay. Practical implementation, however, needs to address the complexity of in-cell dual power rail physical design and problem of power domain isolation. These challenges have hindered the widespread acceptance of fine-grained multi-power domain system design due to considerable area penalty and added design complexity.

Fortunately, recent advance in monolithic 3D integration technology [12] [13] [14] may lead to a fundamental breakthrough in reducing overhead of the multi-power domain system design. The small monolithic inter-tier vias (MIVs), which is similar to normal interconnect via, provide high speed and high-density interconnection between different tiers. Implementing in monolithic 3DIC, the in-cell power rails can be naturally separated and managed in different tiers, greatly simplifies the physical layout design than in conventional 2D IC.

In this study, we propose a novel cross power domain interface (CPDI) circuit, which transfers synchronous data between power domains effectively and reliably. Our CPDI circuit utilizes the level conversion flip-flop (LCFF) structure, and resolves the isolation problem by using a dif-
ferential pair of common source nMOS in the data path between the master and slave stages of the LCFF. Self-induced power collapsing (SIPC) technique [15] is further introduced to enhance level shifter efficiency and reduce conversion power. Moreover, the transistors in the level shifter stage are sized such that it minimizes footprint and achieves reliable data transfer simultaneously. The proposed CPDI is implemented in a dual-tier 3DIC. The two power rails of the CPDI circuit are readily arranged in two separate tiers. Taking the advantages of our novel circuit topology and monolithic 3DIC implementation, we achieved a highly compact, highly reliable, low power CPDI design. Compared with previous cross domain data transfer interface circuits, our optimized CPDI shows a 20%-35% delay improvement and 20%-30% energy saving. To assure design robustness, the proposed CPDI was simulated at 10% power supply bounce and passed the robustness test. To our knowledge, this is the first time that a practical CPDI circuit is designed and implemented in monolithic 3DIC. The implementation in 3DIC is also essential for cross tier, cross domain synchronized data transfer in future multi-power domain 3DIC systems. In the following of this paper, we will introduce the monolithic 3D technology in section II. The detailed CPDI circuit design will be provided in section III. We will show the experimental results in section IV and conclude our work in section V.

II. Monolithic 3D Technology

The monolithic 3D IC is fabricated by stacking high quality monocrystalline silicon layers using low temperature oxide bonding, followed by low temperature transistor and interconnect integrations, sequentially. Connections between tiers are made by monolithic inter-tier vias (MIVs). The process is effectively the same as fab front-end and back-end integration flow, using similar mask alignment technique and CD control. This way, MIV size can be made as small as regular interconnect vias. The layout overhead of MIV is very small and its electrical properties can be simply modeled as a wire with parasitical RC.

MIV allows gate level inter-tier partition that will greatly changes the chip organization methodology. Long wire delay can be reduced by folding a 2D IC design into a smaller footprint monolithic 3D stacked IC tiers. Figure 1 is the cross sectional example of a master slave flip-flop design in monolithic 3DIC. The devices on different tiers can have their own power rails. The separated supply networks on each tier may provides independent power domain control and selective power down, allowing find-grain power domain for system power reduction. The fine grain power control needs clamp cell and level shifter between domain boundaries, thus a high speed cross power domain interface (CPDI) design is critical for synchronized data transfer.

![Schematic of basic half latch level shifter](image)

Fig. 2. Schematic of basic half latch level shifter

III. Cross power domain data transfer interface design

A. CPDI circuit and conventional design

Multi-power domain system data transfer needs a fast and low power interface, which provides two functions. One is to control the data flow by synchronized clock, second is to create full Vddh swing utilizing level shifter. The design target of a level shifter is to quickly transfer data from low voltage domain to high voltage domain and block any possible DC current. The conventional level shifter design (Figure 2) is a cross-coupled pMOS structure (CCLC) [10], which could pull the output to full Vddh swing. Connecting a normal flip-flop and such level shifter together composes the basic cross power domain data transfer circuit. However, such implementation leads to large area, long clock to Q delay, and high switching power.

Since the level shifter itself has cross-coupled structure keeping the data, it is possible and economic to use it as a loop-forcing latch to replace one of the flip-flop stage. In this work, the level shifter is implemented in the slave stage, while the master stage uses a conventional loop-breaking latch.

B. Design Details and Consideration

The proposed CPDI circuit has a write enhanced SRAM-based (WES) structure with self-induced power collapsing (SIPC) technique Figure 3. The setup/hold time of the design mainly depends on the conventional master stage, and the clock-to-q mainly depends on the level shifting stage and the internal clock buffer. There is no DC current path between two power domains, therefore this voltage tripping free design has no feedback from Vddh domain to Vddl domain.

The function of the CPDI circuit is a rising edge trigger flip-flop, which has Vddl swing input and Vddh swing output. When the clock is low, the data signal goes through the master stage pass gate and store the data in master stage node msnd and its reverse value in msnd_n. N1 and N2 controlled by msnd and msnd_n will pull one of their drain nodes to ground, and make the other nMOS drain floating. The slave stage is disconnected to master stage by two clock controlled nMOS (N3 and N4). The output
now is the data stored in the SRAM internal node. When the rising edge comes, the master stage pass gate is off and both \textit{msnd} and \textit{msnd\textsubscript{n}} value are maintained by the clock controlled coupled inverters. The slave stage clocking nMOS is on, and the corresponding SRAM cell side will be written by the pull down path and other side of the SRAM cell will store a Vddh data. The waveform of important circuit nodes are illustrated in Figure 4.

The slave level shifter stage uses a symmetric design. The key part is a custom designed SRAM cell. Normal SRAM cell needs to balance both the read/write margins. However, our design is only sensitive to the write margin and static noise margin when word line is closed. Therefore, we use the WES sizing to speedup the circuit and save dynamic power. During the writing stage, two clocked nNOS pass gates (N3 and N4) are on and the pulling down nMOS (N1 or N2) will compete with the pull up internal pMOS. Thus a WES design has small device size coupled inverters and large device size on the pull down paths.

In order to further decrease the clock to Q delay and improve the pull down path strength, we use a minimum size always on header pMOS (P1) to increase the pull up path impedance by one stack. During level conversion, the current go through coupled pMOS will be provided by the header P1, which will cause a considerable voltage drop from Vddh to Vdd local at internal supply node S. As in Figure 4, this SIPC effect could reduce local power supply to 75% - 80% percent during the transition. The target Vddl/Vddh ratio is around 0.7 for optimal power efficiency [10].
C. Partition and Layout Balancing

The dual-tier CPDI logic structure is shown in Figure 5 exploiting monolithic 3D technology. The Vddl power island is on tier 0 and Vddh power island is on tier 1. It is a single power rail design for each tier. For multi-power domain design, most of the standard cells only work in one power domain and have one power rail. Dual-power rail design of LCFF will significantly decrease the place and route flexibility and increase the design complexity. Our monolithic 3D based design does not have this problem.

The partition of this CPDI circuit into tiers has two considerations: power domain isolation and cell footprint. Two tiers have separate power rails, so that transistors connected to different Vdd supply must be placed in the correspondent tier. Other transistors, like pass gates, are placed to either tier that provides less footprint.

Considering the above two criteria, we partition the master stage and clock buffer into tier 0, and the level shifting slave stage into tier 1. The transistors on each tier are placed such that the overall transistor widths in each tier are close to maximize 3DIC are utilization. Thus, this design has compact layout and make full use of vertical interconnecting resource.

IV. Experimental Results

The proposed WES-SIPC design is implemented in a 45nm channel length low power technology. It has two tiers that contain active devices. Signals are communicated between the two tiers through MIVs. A MIV has similar electrical properties as a normal via between metal layers and thus treated according in the schematic. This is different from TSV based multi-tiers designs, where the TSV capacitance is large. The WES design is placed across two tiers with different power rails. The high voltage domain uses a 1.1V supply, and the low voltage domain uses a 0.8V supply. The size of transistors are optimized for clock to Q delay, under the condition that inputs come from the lower voltage domain and outputs are sent to the high voltage domain.

A. Performance and Energy Evaluation

Timing and energy of the new designs are compared with two other LCFF structures MSHL and MSCC reported in [10] [11]. A baseline structure that is constructed by a flip-flop and a separate CCLC [12] is also studied. The flop is placed in the low voltage domain and the CCLC shifts the flop output to the high voltage domain. The transistor sizing among designs follows the rules below for fair comparison. The sizes are identical for the master stage of the flip-flop and the local clock drivers. The device size of the slave stage are slightly modified in each design to ensure proper level shifting function. The pull-up and pull-down path strength at the level converting nodes are carefully tuned to assure correct function under worst case voltage differential. The output stage uses a FO4 loaded inverter to mimic practical output strength.

The clock to Q delay of all 5 designs are compared in Figure 6. The values are averaged between the output rise/fall cases. The WES-SIPC structure has the best delay, which is around 80% of the MSHL structure proposed in [10]. The delay value of WES w/o SIPC effect is similar to MSHL. The header PMOS weaken the pull-up path of the level shifter during state changes, thus speed up the 1 to 0 transition by 30% in the corresponding node. For the output falling case, bit has 1 → 0 and bit,n has 0 → 1 transition. There are three gate delays from clock rising to output. Although the pull up path for bit,n is weakened, the delay improvement from clock rising to bit falling is larger comparing with the deterioration of bit falling to bit,n rising delay. This clock to Q falling transition also benefits a little from SIPC effect.

Energy consumption and leakage power is normalized to their maximum value in each group and shown in Figure 7. Energy is measured for both output rising and falling cases at a clock period of 2 ns and data activity of 50%. It considers the total energy consumption at Vddl and Vddh power domain and includes the leakage power during the clock period. The trend for energy is similar to the clock to Q delay data. The energy of WES-SIPC design is 80% of the same structure w/o SIPC effect. The flop+shifter design surprisingly consumes less energy than the MSHL structure, but it is still worse than the WES structure with SIPC effect.

Leakage power is measured at both power rails. The total leakage is compared in the light color bar of Figure 7. The WES w/o SIPC design has the same leakage as the one
The setup and hold constraints are compared in Figure 8. Setup time is measured from D to clock. Hold time is measured from clock to D. They are measured by the clock to Q delay. The hold time bars in the plot use a reversed vertical axis, so that the height difference between the setup and hold bars show the length of the timing window that data cannot change. This difference is shown as the gray area in each bar. The WES-SIPC structure has similar setup/hold as the FF+shifter design. It is because their master stages are identical and all the master stage signals are connected to the gate of the slave stage transistors. Without SIPC, constraint timing is not optimized in WES design due to longer state transition time. Applying SIPC technique resolves the problem, making constraint timing competitive to the full optimized FF. The MSHL design uses a nMOS to connect one of the level shifter nodes to the master stage coupled inverter. This requires the data to be stable for a longer time before and after the clock edge.

The energy delay product (EDP) of the five designs is compared in Figure 9. They are normalized to the EDP of the MSCC design that has the maximum value among all designs. The WES structure achieves 45% EDP of the maximum EDP design. Its EDP is only 60% of the FF+shifter design. The use of 6T SRAM structure with SIPC effect greatly improves the slave stage from previous LCFF designs and also reduces the interaction between the two stages.

The area of these designs are listed in Table I. The circuit layouts are designed for standard cell style P&R, whose area are counted by poly tracks. The footprint of our WES type designs utilizing monolithic 3DIC is 6 tracks on each tier. The total chip area of two layers are 12 tracks, which has the same area as the MSHL design. They only uses 75% of the conventional FF+shifter design area. Table I also summarizes the timing, energy and EDP data discussed above.

B. sensitivity to vdd fluctuation

In the proposed design, a level shifter is implemented inside the slave stage of a flip-flop. It uses the loop forcing mechanism, which is different from the commonly used loop breaking mechanism in single voltage domain flops. The clock to Q delay changes with the supply voltage fluctuation at any of the two power domains. We evaluate the WES-SIPC structure clock to Q delay under ±10% voltage bounces on either Vddh or Vddl, which are centered at 1.1 V and 0.8 V, respectively.

The influence of Vddl domain voltage fluctuation is shown in Figure 10. The clock to Q delay of the new WES-SIPC design is better comparing with the conventional FF+shifter design. Around 0.8 V supply voltage of Vddl, the WES-SIPC design changes -0.5 ps/mV responding to Vddl fluctuation. The FF+shifter design has -1 ps/mV response coefficient. The FF+shifter design has more transistors in the Vddl domain, thus it is sensitive to Vddl voltage changes. The gap between the two curves becomes larger at lower voltage region, indicating that performance degradation is smaller for WES-SIPC design.

Change in Vddh domain supply voltage affects the speed...
of level conversion in the slave stage. Figure 11 shows the WES-SIPC design clock to Q delay under ±10% Vdda variation around 1.1 V. The Q rising delay becomes shorter at higher supply voltage. The response coefficient is -0.05 ps/nV. In this transition, the bit_n node is pulled down by two NMOS. With the help of the P1 header transistor, the pull down process becomes faster at higher voltage. The Q falling delay slightly increases at higher Vddh, the slope of the curve is 0.04 ps/nV. The pull up path at the bit_n node is weakened, although the pull down speed at bit node is faster. In summary, the delay difference between output rising and falling becomes smaller at higher Vddh voltage. Comparing the data in Figure 10 and Figure 11, the clock to Q delay variation caused by Vddh fluctuation is much smaller than that caused by Vdd fluctuation.

V. Conclusion

In this work, we proposed a cross power domain interface for data transfer. This interface is constructed by a Master-Slave flip-flop with a level shifter functioned as its slave stage. The level shifter uses the 6T SRAM structure, with special size optimization for write operation. A Self-Induced Power Collapse technique is applied on the SRAM cell to further improve performance and reduce switching power. Comparing with previous designs, our CPDI improves both the performance and the energy consumption by 20-30% under almost the same or smaller footprint and a 60% lower leakage. The implement of our design utilizes monolithic 3D technology, which not only provides the low overhead single power rail structure on each tier, but also increase the flexibility of multi-power domain design. We evaluate the influence of power supply fluctuation for the CPDI circuit clock to Q, which shows better robustness comparing with the FF + level shifter design.

REFERENCES