Analysis and Mitigation of Lateral Thermal Blockage Effect of Through-Silicon-Via in 3D IC Designs

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Abstract—The three-dimensional integrated circuits (3D ICs) offer performance advantages thanks to the increased bandwidth and reduced wire-length enabled by through-silicon-via structures (TSVs). Traditionally TSVs have been considered to improve the thermal conductivity in the vertical direction. However, the lateral thermal blockage effect becomes increasingly important for TSV via farms (a cluster of TSV vias used for signal bus connections between layers). TSV farms can cause different thermal effects on different layers due to the unequal x,y,z thermal conductivities. This can exhibit itself as thermal improvement in the vertical heat flow, at the same time lateral heat blockage effects in thickened pass-through layers. In this paper, we propose a thermal-aware via farm placement technique for 3D ICs to minimize lateral heat blockages caused by dense signal bus TSV structures. By incorporating thermal conductivity profile of via farm blocks in the design flow and enabling placement/aspect ratio optimization, the corresponding hotspots can be minimized within the wire-length and area constraints.

I. INTRODUCTION

Three-dimensional integration offers a number of benefits for future VLSI design [1]. Increased interconnectivity is considered as a key advantage in improving performance by leveraging the high-bandwidth and low-latency through-silicon-via (TSV) structures.


Recent studies showed that 3D integration exacerbates the on-chip temperatures due to the higher transistor density per cooling area and the increased vertical resistances. TSVs have been considered to help drain the heat in the vertical direction [5]. As a result, thermal vias have been employed during placement and routing of 3D ICs to help the vertical heat conduction [6] [7].

However as the TSV scaling continues in advanced 3D technologies, the metal-to-insulator ratio and the distance between TSVs become smaller. While the vertical conductivity improvement is true for larger thermal vias, small and dense signal vias can act as thermal blockages to the neighboring blocks in thin silicon. The lateral thermal-blockage effects of TSV clusters (via-farms) become more prominent and can have a significant impact on the chip thermal profile. (Figure 1(a) shows an illustrative case where a heavily interconnected SOC IP block is surrounded with TSV-farm structures).

For most 3D partitioning approaches 3D floorplanning is usually the first step in the physical design flow [1]. In the current 3D design flow thermal blockage implications of through-silicon-via structures are not taken into consideration. The majority of the existing studies on thermal-aware 3D floorplanning methodologies [8]–[11] have mainly focused on the thermal effects of stacking functional units or IP cores, and some consider enhancing the vertical thermal conductivity with the help of thermal vias. TSVs may have different effects on different device layers in the stack and their conductivities are highly dependent on the technology and design parameters. Current design tools are oblivious to the thermal conductivity range and differences of dense via farms in x,y,z directions. For instance a 3D bus can improve the vertical heat flow (in z direction), at the same time it can also create thermal blockages in the lateral (x,y) direction in the layers that it passes through. This effect can become prominent in dense via farms in thinned silicon. Consequently, in this paper, we study such lateral thermal-blockage effect for TSVs, and make the following contributions:

- We first study the thermal characterization and modeling for the thermal-blockage effects of 3D TSV-farms in unit-level/core-level 3D partitioning (Section III).
- We then propose a thermal-blockage-aware design flow that incorporates a detailed thermal conductivity profile for individual via-farm structures to maximize the heat flow in the lateral and vertical directions (Section IV).

The technique maximizes the lateral heat flow by removing the via-blockages on the heat dissipation paths. TSV-farms are treated as soft macros for temperature flow optimization. The aspect ratio and placement of the via-farm structures can be changed through design iterations in order to improve the thermal profile without causing any performance/area or wirelength degradation. The optimization flow targets maximum performance and minimum wirelength options, while improving the thermal profile at the same time. The proposed technique can improve the performance of temperature-aware floorplanning techniques, by minimizing the exacerbated heating caused by vertical interconnect. As TSVs affect the design flow in multiple device layers, a combination of both inter-layer and intra-layer optimization are needed to effectively deal with such cases. Our experimental results show that the peak/average temperature can be reduced significantly with such thermal-blockage-aware optimization. To the best of our knowledge, this is the first work to study and mitigate the thermal-blockage effects of the 3D TSVs.

II. THE LATERAL THERMAL-BLOCKAGE EFFECTS OF TSVS

![Fig. 1. Thermally optimized 3D TSV-bus (or TSV via farm) structure with enhanced heat flow.](image)

While providing additional advantages over 2D counterparts, 3D...
buses require further analysis and optimization as a result of the more complex interaction among performance, power and temperature characteristics in 3D. Traditionally, such TSV buses have been considered to help improve the thermal conductivity in the vertical direction, with the general perception that Copper/Tungsten TSVs have good thermal conductivities [5]–[7]. However, the lateral thermal-blockage effects for TSV via farms have not been well-studied in the past. A number of factors contributing to the TSV lateral heat blockage effects are:

- **TSV Technology.** Large copper TSVs (with diameters in tens of microns) have been shown to improve the vertical heat dissipation as in thermal vias; However, dense and insulated tungsten via farms with few micron diameters exhibit different thermal characteristics. They can even act as thermal blockages in the lateral direction in thinned device layers. In advanced 3D technologies the sizes and pitches of such through-silicon-vias can be as small as a few microns. While this density can be leveraged towards performance, the resulting thermal behavior deteriorates with smaller metal/insulator ratio and TSV-to-TSV distances. In particular, the electrical insulation in the TSVs has thermal insulation effect in the lateral direction due to the nature of the materials used for insulation. Such lateral thermal blockage effect can be even more serious in the unit-level and core-level 3D floorplanning, where the signal buses among units or cores are implemented as dense TSV via cluster (or TSV via farm).

- **3D Wafer Thinning.** In a 2D setting silicon layer thickness is frequently around 700 – 800µm, which enables effective heat dissipation in lateral and vertical direction in the silicon. The existing temperature gradient between Block A and Blocks B/D in Figure 1(a) can be easily reduced thanks to the lateral heat dissipation in the x/y directions in a 2D architecture. However, in 3D IC design, aggressive wafer thinning is usually needed to reduce the TSV via size and pitch while maintaining the TSV aspect ratio. For example, in 3D stacked IC, the thickness of a wafer can be in the range of 10 – 100µm [1]. As a result, the lateral heat conductivity to the neighboring blocks is greatly diminished. The lateral heat gradients as well as hotspots are exacerbated. Such thermal implications may not be of serious concern for designs with uniform power density and relative low power dissipation such as DRAM layers, however, the higher power processor or accelerator architectures are affected by the localized heating in the thinned processor layers. Hence we focus our attention to the microprocessor stacks with local power density variations within the layers.

Figure 2 shows illustrative case of a dense TSV farm implementation with silicon measurement via on-chip thermal sensor placement, where the TSV-farm have different characteristics. Compared to Figure 2 (b), the via-farm area in Figure 2 (c) creates a blockage to the heat flow due to the lower conductivity of the via-structures in addition to the electrical insulation. The local hotspot exacerbates, also the span of the hotspot area has expanded as shown in the corresponding thermal map.

Such lateral thermal-blockage effects of TSV via farms can have significant impact for the coarse-granularity 3D SoC design or 3D multi-core design, with either unit-level or core-level partitioning:

- **Unit-level Case:** At the unit-level, the temperature differences are frequently large due to the inherent characteristics of the underlying structures. Recent studies have shown heavily interconnected structures such as instruction scheduling units, register files and integer/ floating point execution units as frequent hotspots within the core. Such structures have heavy communication demands to the rest of the core, as well as high power densities. In a 3D setting TSV farms surrounding such units can cause increased hotspot temperatures by creating lateral heat blockages.

- **Core-level Case:** At the core-level, temperature differences have been reported to be high where high-activity cores communicate with the other layers through the surrounding TSV farm/bus structures. Since the proximity and placement of bus structures will cause unexpected increases in the hotspot temperatures, even identical workloads can result in different temperature profiles depending on the bus-blockages. This impacts the effectiveness of workload-aware management algorithms as well since such heating is not predictable at system-level.

Thermal behavior of 3D via-farm structures varies significantly with the through-silicon-via size/pitch and material selection in the corresponding 3D manufacturing flow, as well as the specific geometry and placement decisions at the design time. The localized hotspots due to such lateral heat blockage are difficult to predict and can have detrimental effects on not only energy efficiency and thermal profile of the 3D stack but also reliability characteristics. When wide 3D bus structures with dense vias span multiple-layers vertically they can create thermal blockages throughout the 3D stack. Such blockages can affect multiple layers in the stack - even those that are not directly connected to the via farms, which consists of 3D bus signals.

Consequently, with thermal characterization and modeling for TSV buses (via farm) (see Section III), we propose thermal-blockage-aware bus optimization techniques such that the temperature profile of the individual layers as well as the overall stack can be improved. For example, the floorplann of Figure 1(a) can be optimized to help lateral thermal dissipation as shown in Figure 1(b). By identifying the maximum temperature gradients in the layer, the bus structures are removed from these efficient heat dissipation paths. The aspect ratios are adjusted for minimizing the heat blockages in the corresponding directions targeting localized hotspots. As a result, the temperature profile and energy efficiency are improved without compromising the performance advantages of vertical bus structures.

**III. THERMAL CHARACTERIZATION AND MODELING OF 3D TSV-FARM STRUCTURES**

In this section, we present the characterization and modeling of TSV-Farm structure, which are used to guide our optimization techniques that are presented in the next section.
TABLE I

THERMAL CONDUCTIVITIES OF MATERIALS IN 3D ICs

<table>
<thead>
<tr>
<th>Material</th>
<th>Thermal Conductivity (W/(mK))</th>
</tr>
</thead>
<tbody>
<tr>
<td>Copper (TSV)</td>
<td>401</td>
</tr>
<tr>
<td>Tungsten (TSV)</td>
<td>173</td>
</tr>
<tr>
<td>Silicon</td>
<td>149</td>
</tr>
<tr>
<td>Polysilicon</td>
<td>23.1</td>
</tr>
<tr>
<td>Thermal interface material [14]</td>
<td>5.0</td>
</tr>
<tr>
<td>SiO$_2$ (Dielectric / TSV liner [15, [16])</td>
<td>1.38</td>
</tr>
<tr>
<td>Bonding adhesive [17]</td>
<td>0.29</td>
</tr>
</tbody>
</table>

where $k_{farm}$ is obtained from the characterization presented in previous sub-section. $A_L$ and $A_V$ are the cross sectional areas in the lateral and vertical directions, respectively. $\eta_{farm}$ and $\eta_{Si}$ are the ratios of areas each material occupies in the grid cell

IV. THERMAL-BLOCKAGE-AWARE TSV-FARM OPTIMIZATION

In this section we present the design methodology to optimize the thermal characteristics of TSV-farm (3D buses).

A. TSV-farm Optimization Objective

The heat conduction $H_{AB}$ between two units A and B on the same layer can be expressed as:

$$H_{AB} = \frac{\Delta Q}{\Delta t} = k \cdot A \cdot \Delta T/x$$

where $k$ is thermal conductivity of the material, $A$ is the cross sectional area, $x$ is the distance between blocks A and B, and $\Delta T$ is the temperature difference between the units. In this context, the $\Delta Q/\Delta t$ is the rate of heat flow between A and B. When the TSV-farm structures are taken into account, a new metric, which is defined as the heat conduction at a unit temperature difference, is introduced to quantify the heat conduction efficiency with different thermal conductivities:

$$f_{H_{AB}} = \frac{\Delta Q/(\Delta T \cdot \Delta t)}{k \cdot A/x}$$

The heat conduction efficiency $f_{H_{AB}}$ captures the impact of TSV-farm structures on thermal via thermal conductivity $k$ and the geometrical parameters $A$ and $x$. As the cross sectional area $A$ can be reduced significantly (from $700 – 800\mu m$ silicon to $10 – 20\mu m$ silicon), the resulting lateral heat conduction is proportionally affected in thinned silicon. For a given distance $x$ between blocks, our proposed technique improves the heat conduction efficiency $f_{H_{AB}}$ by enabling the heat dissipation along the path with higher thermal conductivity and larger contact area. In particular, the algorithm maximizes the heat conduction efficiency on the maximum thermal gradients, where the temperature distance between the source and drain are highest. By arranging the geometries (in terms of aspect ratio) of TSV-farm structures, along with re-placement, the algorithm improves the thermal profile of chips in the challenging lateral direction.

B. TSV-farm Optimization Flow

The proposed flow optimizes the performance and area driven solution by incorporating temperature awareness. Details of the temperature-aware bus placement flow are illustrated in Figure 4. In the first stage, the initial thermal profiles of the individual units are obtained from design time thermal analysis, along with the vertical interconnectivity among layers in the stack, which indicates the width, source and destination information for the 3D interconnect structures.

The algorithm features two loops of iterations: one at stack level and one at layer level. In the inner loop the algorithm follows a bottom-up layer-by-layer order. In each layer $i$, the algorithm estimates the initial thermal profile, and finds out the TSV-farm structures that start from layer $i$. The TSV-farm structures are treated as soft blocks in the view of floorplanning. A simulated-annealing based floorplanning is then performed, to replace longer/higher aspect ratio bus geometries with wider/square alternatives, as well as moving the bus structures around. A cost function incorporating multiple evaluation metrics is used to guide the floorplanning. After the optimization in layer $i$ is finished, the algorithm enters a new iteration with layer $i+1$ until all layers are optimized. The outer loop then checks whether the average temperature of the whole stack is reduced by the layer level optimization. The algorithm terminates after a given
Start with layer 0.

Start Optimization for Layer i

Temp. Estimate For Units on Layer i

InterOlayer Connectivity For Layer i, i+1, iO1

Find All Neighbor Blocks With TSV Farm Result Between

Calculate Lateral Heat Flow Evaluate Cost Function

Yes, continue with next layer

COST = COST_THRESHOLD

No, continue with layer-level optimization

TSV Farm Aspect Ratio and Shape Change

TSV Farm Other Blocks Placement Change

Simulated Annealing Based Placement

StackOlevel Avg. Temp. Reduction > ∆?

No, iterate with layer-level optimization

Yes, Done

Start with layer 0.

Fig. 4. Details of the temperature-aware vertical interconnect optimization technique.

SAPlacement(S)

▷ Initialization
1. Get an initial floorplan $S_{best} = S$;
2. Get an initial temperature $T > 0$;
3. Simulated-annealing based placement
4. while $T > T_{THRESHOLD}$
5. do for $i ← 1$ to MAX_MOVES
6. do $S' ← \text{GenMove}(S)$;
7. if $\Delta C \leq 0$
8. do $S ← S'$;▷ Down-hill move
9. else
10. $S ← S'$ with the probability $e^{-\Delta C / T}$;
11. if cost($S_{best}$) > cost($S$)
12. do $S_{best} ← S$
13. $T = rT$;
14. Return $S_{best}$;

GenMove(S)

1. Randomly pick up a TSV-farm structure from $S$;
2. Generate a random number $i$ between 0 and 1;
3. if $i < 1/2$
4. do Change the aspect ratio;
5. Recompute the width/height of the TSV-farm;
6. else
7. Change the position of TSV-farm in the floorplan;
8. Recompute the floorplan $S$;
9. Return $S$;

Fig. 5. Outline of the simulated-annealing based placement algorithm.

number of iterations and the floorplannings leading to the maximum overall reduction is recorded.

C. Simulated-Annealing Based Placement of TSV-Farm Structures

A simulated-annealing based floorplanner is employed during the optimization to facilitate the changes of aspect ratio and placement of TSV-farm structures. The outline of the algorithm is shown in Figure 5, which starts with a generic simulated annealing framework (Line 3-13 of the SApIacement routine), and iteratively changes the aspect ratio of TSV-farm structures (Line 4-5 of the GenMove routine) as well as moves the structures around (Line 7 of the

GenMove routine), to obtain a better thermal distribution across the chip.

The cost function used during the placement algorithm (Line 6 and 9 in the SAPIacement routine in Figure 5) is defined as follows:

$$F_{cost} = \alpha \cdot A + \beta \cdot f_H + \gamma \cdot R + \delta \cdot W$$  (6)

where

$$f_H = \sum_{A, B \text{ are adjacent}} f_{H_{AB}}$$  (7)

$$R = |\text{Ratio} - \text{Ratio}_{\text{prefect}}|$$  (8)

where $\alpha$, $\beta$, $\gamma$, and $\delta$ are weighting factors. $A$ is the final floorplan area, $f_H$ is the total heat gradient efficiency involving TSV-farm structures, $R$ is to regulate the overall aspect ratio of the floorplan, and $W$ is the total wirelength.

First, in order to bound the floorplan overhead on silicon area, $A$ and $R$ are included in the cost function. The replacement of TSV-farm structures will also lead to a redistribution of interconnect wires in the metal layers. Therefore, the floorplanner uses a simple wire length model based on Manhattan-distance, to estimate the wire length overhead.

The heat gradient efficiency function is the major metric to guide the floorplanning. As higher efficiency is desired, the weighting factor for the cost contribution of $f_H$ should be negative. For the weighting factors for $A$ and $W$, the values are chosen to be considerably high to impose high penalty on area or wire length overhead. This ensures the TSV-farm optimization with improvements on thermal and negligible overhead on chip area and total wire length.

V. EXPERIMENTAL RESULTS

In this section we show experiment results as well as a case study on the optimization of vertical bus structure (or TSV-farm) in 3D designs with either unit-level or core-level partitioning. Table III lists the technology parameters used in the experiments. The average values in the ranges are used as default, while full ranges are explored for experiments. The thermal evaluation is performed in the modeling infrastructure discussed in Section III.

TABLE III

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSV farm thermal conductivity</td>
<td>0.5 - 5 W/(mK) (Range Explored)</td>
</tr>
<tr>
<td>TSV size/pitch</td>
<td>2 - 5 µm@2x</td>
</tr>
<tr>
<td>Avg. TSVs per core</td>
<td>$10^4$</td>
</tr>
<tr>
<td>Average core area</td>
<td>10 mm²</td>
</tr>
<tr>
<td>Power density</td>
<td>1 - 5 W/mm²</td>
</tr>
<tr>
<td>Silicon thickness</td>
<td>10 - 100 µm thin Si</td>
</tr>
</tbody>
</table>

A. Thermal Optimization Results for Unit-level Partitioning

To quantify the temperature reduction brought by the TSV-farm optimization, we conduct experiments on a set of MCNC benchmarks. The benchmark circuits are partitioned at the unit-level, using a similar approach in [11], to minimize total interconnect wire length as well as the peak temperature. The interconnect information is extracted from the initial floorplan and the TSV-farm blocks are created accordingly.

We then apply the TSV-farm optimization flow on the benchmark circuits, and the results are reported in Table II. Columns 2-3 and 7-8 show the wire length and the chip area before and after the TSV-farm optimization, while columns 4-6 and 9-12 compare three temperature values: the average temperature all over the chip (avgT), the peak temperature (peakT), and the average temperature of the
TABLE II
TSV-FARM OPTIMIZATION ON A SET OF MCNC BENCHMARKS

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Before TSV-Farm Optimization</th>
<th>After TSV-Farm Optimization</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>wire length (µm)</td>
<td>area (mm²)</td>
</tr>
<tr>
<td>am243</td>
<td>346.83</td>
<td>711.65</td>
</tr>
<tr>
<td>am249</td>
<td>346.83</td>
<td>711.65</td>
</tr>
<tr>
<td>alpha</td>
<td>304.72</td>
<td>346.83</td>
</tr>
<tr>
<td>hp</td>
<td>304.72</td>
<td>346.83</td>
</tr>
<tr>
<td>kxroz</td>
<td>304.72</td>
<td>346.83</td>
</tr>
<tr>
<td>Average</td>
<td>304.72</td>
<td>346.83</td>
</tr>
</tbody>
</table>

TABLE IV
THE CHANGES IN AVERAGE TEMPERATURES OF EACH LAYER

<table>
<thead>
<tr>
<th>Avg. Temp. (K)</th>
<th>Bottom Layer</th>
<th>Top Layer</th>
<th>Whole Stack</th>
</tr>
</thead>
<tbody>
<tr>
<td>Before Optimization</td>
<td>323.58</td>
<td>319.87</td>
<td>321.71</td>
</tr>
<tr>
<td>After Optimization</td>
<td>319.06</td>
<td>320.33</td>
<td>319.70</td>
</tr>
</tbody>
</table>

hottest block in the chip, respectively. As shown in the table, on average a 16 K reduction on chip peak temperature and 3 K reduction on chip average temperature are achieved with negligible wire length overhead, and the chip area is slightly reduced due to the re-shape and re-placement of TSV-farm structures. We can see that although the input circuits are already optimized for peak temperature minimization, a significant improvement of thermal profile can still be obtained with the proposed optimization flow, given that the lateral thermal conduction of TSV-farm structures is taken into account.

B. Core-Level Case Study: Multi-Core Stacking

After examining the cases for unit-level partitioning, we perform a set of case studies on 3D bus based architectures at core-level partitioning. Core-level integration is operating at a coarser granularity with much larger silicon area and more intensive use of TSV-farm structures as vertical bus connections.

Figure 6 shows the floorplan of a stacked multi-core architecture used for the first case study. We consider a 2-layer multi-core stack, where each core has its private L2 cache, with a set of vertical bus architectures going (from the I/O pads) through the bottom layer and connecting to the layer immediately on top. Each layer has 6 SPARC-like processor cores with surrounding TSV-farm structures, one shared bus structure BUS0, as well as several blocks for peripheral circuits, as shown in Figure 6. The floorplan of the shown layer is repeated in the top layer.

We first show in Figure 6 the temperature map of the two layers. In the bottom layer as shown in Figure 6(a), local hotspots are formed in the execution units of CORE2 and CORE5. Such a steep temperature gradient across the TSV-farm structures is uncommon in conventional thermal profiles when the lateral heat blockage of TSV-farm is not taken into account. However, local hotspots are not formed near the TSV bus structures in the top layer, because TSV farms in this layer are connected to the metals and the blockage effect is eliminated. The thermal-aware bus structure optimization flow is then performed and the optimization result is shown in Figure 7, where the TSV-farm structures are re-shaped and re-positioned, leading to a slightly different floorplan. From the figure we can see that the local hotspots are migrated with much lower peak temperatures. Note that the average temperatures of the two layers are changing in different directions, as shown in Table IV. The optimization algorithm is able to trade off the improvement in one layer to degradation in the other layer, and to achieve a reduction in the average temperature of the whole stack.

Table V compares the temperature of local hotspots on each core of bottom layer before and after the optimization. Column 2 shows the peak temperature of the chip, while columns 3-8 show the temperatures of the hottest blocks in CORE1-CORE6, denoted by C1-C6, respectively. As shown in the table, the peak temperature is reduced by 12 K thanks to the removal of lateral heat blockage of TSV-farm structures. The average temperatures of the hottest blocks on each core are reduced to different extents, while CORE2 and CORE5 benefit most from the TSV-farm optimization, with their hottest blocks located in the center of the chip and the thermal blockage of both local BUS structures and the shared BUS0 now eliminated.

TABLE V
COMPARISON OF TEMPERATURES BETWEEN CORE-LEVEL HOTTEST BLOCKS BEFORE AND AFTER OPTIMIZATION

<table>
<thead>
<tr>
<th>L1 K1</th>
<th>Peak</th>
<th>C1</th>
<th>C2</th>
<th>C3</th>
<th>C4</th>
<th>C5</th>
<th>C6</th>
</tr>
</thead>
<tbody>
<tr>
<td>Before</td>
<td>346.8</td>
<td>335.8</td>
<td>339.2</td>
<td>335.9</td>
<td>335.9</td>
<td>339.2</td>
<td>335.8</td>
</tr>
<tr>
<td>After</td>
<td>334.0</td>
<td>331.8</td>
<td>332.0</td>
<td>331.8</td>
<td>331.8</td>
<td>332.0</td>
<td>331.8</td>
</tr>
<tr>
<td>Reduction</td>
<td>12.8</td>
<td>4.0</td>
<td>7.2</td>
<td>4.1</td>
<td>4.1</td>
<td>7.2</td>
<td>4.0</td>
</tr>
</tbody>
</table>

To further examine the thermal blockage effect of TSV-farm structures with more detailed information, we zoom in the views in Figure 6 and 7, and focus on the crossing region between CORE1 and CORE4. The detailed thermal profile on block-level of the region is shown in Figure 8, and the temperature numbers are listed in Table VI. As shown in Figure 8(a), the TSV-farm structures BUS1a,
blocks around BUS0a are affected. As a result, IntExec1 becomes a new local hotspot instead of IntReg1. This again shows the significance of the lateral thermal blockage of TSV-farm structures and the necessity of thermal-aware TSV-farm placement optimization.

VI. CONCLUSION

Three-dimensional integration has been shown to provide significant advantages in terms of inter-layer bandwidth and reduced latency. Yet the dense via farm structures of the 3D bus that are used for signal transmission can exacerbate the existing thermal challenges in 3D IC design. Our experimental results show that TSV farms can cause different thermal effects on different layers due to the unequal x, y, z thermal conductivities. This can exhibit itself as thermal improvement in the vertical heat flow in addition to lateral heat blockage effects in pass-through layers. We propose a temperature-aware TSV-farm (3D bus) architecture flow, which minimizes the impact of vertical interconnect, by improving the heat conduction in the lateral direction through via-farm adjustments. Our experimental results indicate the temperature-aware 3D bus flow improves the thermal profile of the 3D IC designs.

REFERENCES