Low-power Dual-element Memristor Based Memory Design

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ABSTRACT

Recently, the emerging memristor device technology has attracted significant research interests due to its distinctive hysteresis characteristic, which potentially can enable novel circuit designs for future VLSI circuits. In particular, characteristics such as non-volatility, non-linearity, low power consumption, and good scalability make memristor one of the most promising emerging memory technologies. Some important design parameter, however, such as speed, energy consumption, and distingushiablility, are mainly determined by the memristor's physical characteristics. In this paper, a key observation of memristor's asymmetric energy consumption is made by the detailed analysis of the transient power consumption. Based on this observation, we propose a dual-element memory structure in which each memory cell consists of two memristors. By constantly writing complement bits into the two elements within a cell, the dual-element is flexible to satisfy design constraints which are usually difficult to be satisfied with one-cell memory structure. Design space of the dual-element memory cell is studied and it shows that the trade-offs among the energy, speed, and distingushiablility should be explored for different design objectives. In particular, we show that under the energy-driven optimization, the proposed dual-element memory achieves the same programming speed and distinguishability as conventional single-element memory but the energy consumption can be reduced by up to 80%.

Categories and Subject Descriptors

B.7.1 [**INTEGRATED CIRCUITS**]: Types and Design Styles—*Memory technologies*

General Terms

Design, Measurement

Keywords

Memristor, Low Power, Nonvolatile Memory

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1. INTRODUCTION

Memristor, known as the fourth basic circuit element, was first theoretically predicted by Chua in 1971 [1], and practically demonstrated by HP Labs in 2008 [2]. This emerging technology has many attractive features, including non-volatility, non-linearity, low-power, and good scalability. Such properties grant memristor the potential for innovations for future circuit and system architecture designs. For example, as memristor can accomplish most of the behaviors of the synapse such as remembering the past dynamic history and storing a continuous set of states, it has the potential to realize electronic neural networks [3] [4]. Some practical approaches of analog circuits with memristor have been proposed based on its non-linearity property [5] [6] [7]. In addition, non-volatility and good scalability make memristor a promising candidate as the next-generation high-density, high-performance memory technology [8], and it has been predicted that memristor-based memory will be a strong competitor against other emerging memory technologies such as phase-change memory (PCRAM) and Spin-Torque-Transfer Magnetic memory (STT-RAM) [8] [9].

For memory design, reducing the energy consumption is one of the most important design metrics for both high-end computing applications or low-end embedded applications. In this paper, we perform a comprehensive study to analyze the power and energy consumption of memristor-based memory design which adopts HP's thin-film memristor technology [2]. Based on the observations from our analysis, we propose a novel dual-element memristor based memory structure. In this novel structure, each memory cell contains two memristors, within which the complement bits are stored. During the read operation, the differential signals will be read out, and converted to logic '0' or '1'. By writing complement bits into the two elements within a cell, the dual-element is flexible to satisfy design constraints which usually cannot be achieved by one-cell memory structure. Design space of the dual-element is studied in this paper and it shows that a trade-off among the energy, speed, and distingushiablility should be explored for optimization of different objectives.

2. PRELIMINARIES

2.1 Memristor Model

The memristor is formally defined as a two-terminal element in which the magnetic flux between the terminals is a function of the amount of electric charge q that can pass through the device, which is explicitly expressed by the

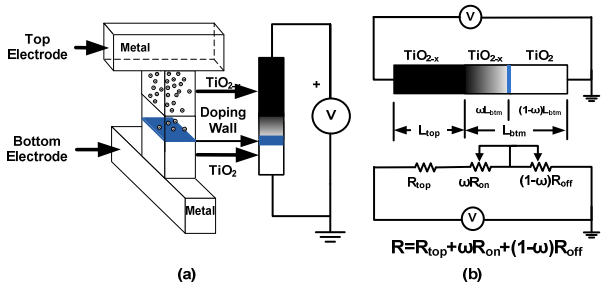


Figure 1: Structure and model of memristor cell

equation $d\varphi = Mdq$, where M is called the memristance. If the relation is linear, memristance becomes constant and the memristor acts as a resistor. By contract, if it is non-linear, the memristance varies with the charge, which determines the hysteretic behavior of current/voltage profile, and can be defined as $M(q)$. Generally, a memristive system can be described by the following relations:

$$\begin{cases} V(t) = M(\omega, i, t)I(t) \\ \omega = f(\omega, i, t)\ , \end{cases} \tag{1}$$

where ω is the variable that indicates the internal state of the memristive system, $V(t)$ and $I(t)$ denote the voltage and current across the memristive system. Note, M is the memristance and depends on the system state, current, as well as time. If the memristance in Equation (1) only depends on the cumulative effect of current, it becomes a charge dependent device, and is called a current-controlled memristor.

The structure of HP's memristor cell is shown in Fig. 1(a) [2]. In this metal-oxide-metal structure, the top electrode and the bottom electrode are two thick metal wires on Pt, and two titanium dioxide films are sandwiched by the electrodes. The upper titanium oxide is doped with oxygen vacancies, noted as TiO_{2-X}, and has relatively high conductivity as a semiconductor. The lower oxide, which is perfect titanium oxide without dopants, has its natural state as an insulator. When a biased voltage is applied cross the thin film, the oxygen vacancies are driven from the doped oxide to the undoped oxide and consequently lower the memristance of the whole cell. Contrarily, with a reversed bias voltage, the dopants migrate back to the doped oxide.

Based on the dopant drifting characteristics, the memristor can be modeled as a two-terminal device, which is made up of three resistors in series. Fig 1(b) shows the schematic of memristor model. The thicknesses of the upper and bottom oxides are L_{top} and L_{btm}, respectively. The upper oxide has a constant resistance of R_{top}. But the resistance of the bottom oxide depends on the status of the oxide. We can denote the full undoped resistance as R_{off} and the full doped resistance as R_{on}. Obviously, R_{top}, R_{on}, and R_{off} has the relationship as: $R_{off} \gg R_{on}$, $R_{off} \gg R_{top}$, and $R_{top}/R_{on} = L_{top}/L_{btm}$.

Since R_{top} is a constant and relatively small, the total resistance is predominantly determined by the status of the bottom oxide. The state variable ω is defined as the proportion of the length of the doped region to the total length of the bottom oxide, as shown in Fig. 1(b). Thus, the mathematical model for the memristance of the cell can be described by the resistances and the internal state ω as [2]:

$$M(\omega) = R_{top} + \omega R_{on} + (1-\omega)R_{off}\ , \tag{2}$$

Under a biased voltage $v(t)$, the length of the doping region will change, which results in the change of the state variable ω. For example, a positive voltage causes the dopants (oxygen vacancies) to drift to the undoped region and therefore result in a lower memristance of the whole memristor. In the linear drift model, the boundary between the doped and undoped region drifts at a constant speed as: $v_{drift} = \mu_v R_{on} i(t)/L_{btm}$. Based on this fact, the memristor can be modeled as [2]:

$$\begin{cases} v(t) = (R_{top} + \omega R_{on} + (1-\omega)R_{off}) \cdot i(t) \\ \frac{d\omega}{dt} = \frac{\mu_v \rho_{T_i O_{2-x}}}{LS} i(t) \end{cases} \tag{3}$$

and the internal state (ω) can be deduced as:

$$\omega(t) = \frac{\xi_1}{\xi_2} - \sqrt{(\alpha_0 - \frac{\xi_1}{\xi_2})^2 - \frac{\lambda}{\xi_2}\varphi(t)}\quad , \tag{4}$$

where $\xi_1 = R_{off} + R_{top}$, $\xi_2 = R_{off} - R_{on}$, and $\lambda = 2\mu_v\rho/LS$. Also, α_0 denotes the initial state of the memristor. Since the parameters ξ_1, ξ_2 and λ are constants and only depend on the material and manufacture process, the internal state ω can be considered as a flux-driven variable. Accordingly, the memristance is determined by the flux applied to it, regardless the waveform of the input voltage. Considering the flux is the integral of voltage on time, if a square wave pulse is applied to the cell, the change of the memristance consequently depends on the pulse width of the input voltage. In this case, these properties make it suitable to employ memristor as a voltage-driven memory cell.

2.2 Memristor-based Memory

Attractive properties of the memristor such as non-volatility, high distinguishability, low-power, scalability and fast accessing speed make it a promising candidate for the next-generation high-density and high performance memory technology [8][10]. Consequently, memristor-based memory structure has been studied recently [8]. The basic structure of memristor-based memory is very similar to a typical memory array such as SRAM-based and DRAM-based memory, which consist of the word line decoder, memory array, sense amplifier and output MUX. However, due to the special electronic characteristics of memristor, several additional peripheral circuits, such as pulse generator and R/W selector, should be added to implement the write/read operations. With the non-volatility and the flux-driven properties, the key features for the memristor-based memory can be summarized as follows:

1) **Information Storage:** It has been reported that the off-to-on resistance ratios of HP's memristor can achieve as much as 1000 [11], which implies a good distinguishability of the memristor-based memory. Since the memristance can reflect the internal state ω of the memristor, we can define the high resistance as logic '0' and the low resistance as logic '1'. In addition, in the presence of noise, a safety margin should be defined to ensure the reliability of the cell.

2) **Write Operation:** The write operation is to change the internal state of the memristor and therefore change the information stored in the cell. A simple way to write the memristor is to apply enough positive (writing logic '1') or negative (writing logic '0') voltage to the memristor cell. By applying a square wave pulse to the cell, the net flux is only determined by the polarity and pulse width of the input

voltage. Thus, one can carefully adjust the input voltage to ensure the correct write operation.

3) **Read Operation:** The read operation is more complicated than the write. To read a memristor cell, a voltage is applied across the cell and the current is converted to voltage output by a sense amplifier. Besides, in order to avoid the disturbing read and ensure the stabilization of the memristor's internal state, a two-state read operation is proposed in [8]. The read pattern contains a negative pulse and a positive pulse with the same magnitude and duration, makeing sure zero net flux is imported into the memristor cell.

4) **Refresh Scheme:** If the waveform of the read operation is not perfectly symmetrical, the net flux applied to the memristor becomes nonzero. After several read operations, the accumulative net flux disturbs the internal state significantly and result in soft errors. Thus, given a boundary of the mismatch between negative and positive pulse widths, a refreshing operation is needed to refresh the internal state after every specific number of read operations.

The recently proposed memristor-based memory array structure design used the crossbar structure [8]. In such crossbar-based memory structure, a diode in series with data storage cell is used as the selector of the cell. Such structure can works well for the unipolar memory cell. However, for a bipolar device as memristor, it is difficult to provide a method to select a memristor in a crossbar array without disturbing the adjacent memristors, and such method can result in significant leakage current for the memory array [12] [13]. Consequently, in our design, we follow the traditional memory structure and use MOSFET as the selector of the memory cells. However, this design methodology can be easily used in cross-bar based memristor memory array as long as the appropriate non-ohmic selector is discovered.

3. MEMRISTOR-BASED DUAL-ELEMENT MEMORY DESIGN

In this section, we first characterize the power/energy consumption of a memristor cell. Based on our derivations, we propose a low-power dual-element memristor-based memory structure. The circuity for the dual-element memristor-based memory is also described.

3.1 The concept of dual-element memristor cell

One of the most distinguished features of memristor is that its internal state is only determined by the initial state (ω_0) and the accumulated flux (φ) applied to it, which is shown in Equation (4). Besides, Equation (2) shows that there is a one-to-one correspondence between the internal state (ω) and the memristance (M). Therefore, from Equation (2) and Equation (4), the memristance of a cell is solely dependent on the flux as:

$$M(\varphi) = \sqrt{(\xi_1 - \alpha_0\xi_2)^2 - \lambda\xi_2\varphi} \quad , \tag{5}$$

Based on this observation, if a constant voltage, V_{in}, is applied to the memristor, the current-voltage relationship can be described as:

$$i(t) = \frac{V_{in}}{\sqrt{(\alpha_0\xi_2 - \xi_1)^2 - \lambda\xi_2 V_{in} t}} \quad , \tag{6}$$

From the model presented in Equation (2), the lower bound and upper bound of the memristance are $R_{top} + R_{on}$ and $R_{top} + R_{off}$. Thus Equation (6) is valid during the time

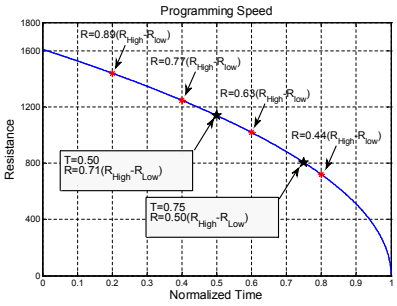


Figure 2: Programming Time vs Resistance

interval of:

$$\frac{-2\alpha_0\xi_1 + \alpha_0^2\xi_2}{\lambda V_{in}} < t < \frac{2(1-\alpha_0)\xi_1 - (1-\alpha_0^2)\xi_2}{\lambda V_{in}} \ . \tag{7}$$

Otherwise, the currents are $i_{max} = V_{in}/(R_{top} + R_{on})$ and $i_{min} = V_{in}/(R_{top} + R_{off})$, respectively.

Assuming that the programming time stays in the valid interval defined in Equation (7), the power and energy consumption can be calculated as:

$$\begin{cases} P(t) = \frac{V_{in}^2}{\sqrt{(\alpha_0\xi_2 - \xi_1)^2 - \lambda\xi_2 V_{in} t}} \\ E(t) = \int_0^t P(x)dx \\ \qquad = \frac{2V_{in}}{\lambda\xi_2}((\xi_1 - \alpha_0\xi_2) - \sqrt{(\xi_1 - \alpha_0\xi_2)^2 - \lambda\xi_2 V_{in} t}\ ) \end{cases} \tag{8}$$

Note that in Equation (8), the second part in the brackets has the same expression as the memristance shown in Equation (5), meaning that from the same state α_0, the energy consumption is only determined by the final memristance after the write operation. Therefore, if we do not use the whole range of the resistance, and only program a part of the memristor, the energy consumption can be saved remarkably. With this partial programming, the write pulse width is also reduced, and hence the write speed is increased. As shown in Fig. 2, the time for programming the cell from R_{High} to $\frac{1}{2}(R_{High} - R_{Low})$ is reduced to 75% of the original time. On the other hand, if we program the cell from R_{Low}, the programming time is reduced to 25%. Intuitively, programming the low resistant part of the memristor is faster than programming the high resistance part. Therefore, we can take advantage of this kind of "partial programming" to optimize the memristor-based memory.

One obvious limitation of partial programming is that the distinguishability of the memristor cell is reduced. The distinguishability of a memory cell is the ability to distinguish logic '0' and logic '1' during the read operation. For a memristor-based memory cell, the read operation is realized by applying a small voltage across the cell and then sensing the current through the cell. Since the magnitude of current is determined by the resistance of the memory cell, to ensure the reliability of the read operation, current accessing the cell should be distinguishable enough. As a result, the ratio of high resistance to low resistance can reflect the distinguishability between logic 0 and logic 1. For our memristor model, this ratio, $Ratio_M$ can be calculated as:

$$Ratio_M = \frac{R_{high}}{R_{low}} = \frac{\xi_1}{\xi_1 - \xi_2} \ . \tag{9}$$

It is important to notice that $Ratio_M$ is the physical parameter of a memristor cell and only determined by the storage

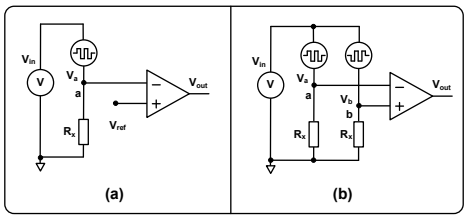


Figure 3: Sense scheme for single-/dual-element memristor-based memory cell

material. If we also consider the sense scheme of the cell, which is shown in Fig. 3(a), the distinguishability of the cell is determined by the voltage gap applied to the sense amplifier. Under an input voltage V, the voltage applied to the sense amplifier is: $V_{out} = V_{in}R_x/(R_x + R_{cell})$. Given the high resistance R_{high} and low resistance R_{low}, the series resistor R_x should be selected carefully to achieve the maximum voltage difference. This 'optimal' value of R_x is: $R_x = \sqrt{R_{high}R_{low}}$. Therefore, the maximum voltage difference applied to the sense amplifier, defined as Λ, can be determined by:

$$\Lambda = \frac{V_{in}}{2} \cdot \frac{R_{high} - R_{low}}{(R_{high} + R_{low}) + 2\sqrt{R_{high}R_{low}}} \quad . \tag{10}$$

If partial programming is applied to the cell, both $Ratio_M$ and Λ are reduced, which results in a degradation of the distinguishability of the cell. To overcome this disadvantage, a dual-element memristor-based memory is proposed. The basic idea of the dual-element memory cell is to use a pair of memristors to store the differential signals of the input data. During the write operation, the differential signals are saved in the cells separately. One of the cells, named the positive cell, stores the data with the same polarity of the input data, while the other one, negative cell, stores the complementary data. For example, in order to write logic '0' into the cell, the positive cell is written to high resistance. At the same time, the negative cell is written to low resistance. The read scheme is different from the general memristor memory proposed in [8]. As shown in Fig. 3(b), during the read operation, instead of comparing the voltage to a reference resistance, the voltages from the two memristors are compared. Therefore, the voltage gap input to the sense amplifier is also increased. In order to obtain the same voltage gap, the memristor should be programmed to the statu that: $R_{int} = \sqrt{R_{high}R_{low}}$. In this way, we can partial program each of the cell separately and use the associated information to achieve enough distinguishability.

3.2 Design space exploration

As mentioned above, the partial programming is faster than full programming. Also, the change of memristance is only determined by the flux applied to the memristor. For energy optimization under a specific performance constraint, we can apply a low-magnitude long-width voltage pulse to program the cell. According to Equation (8), the energy consumed in the write operation is reduced as the input voltage decreases. On the other hand, one can also optimize the performance of the memory array under a specific energy constraint. Consequently, to design a dual-element memristor-based memory cell, the trade-offs among speed, energy, and $Ratio_M$ should be carefully explored. In order to

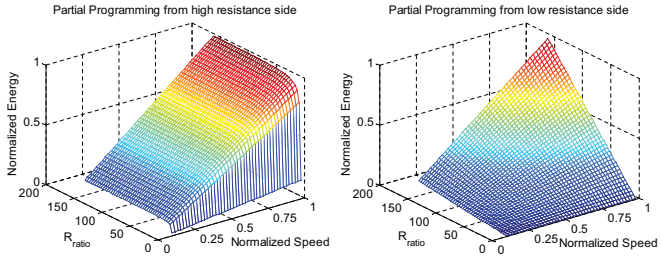


Figure 4: Design space of dual-element cell

explore the design space for dual-element memristor-based memory, the following constraint should be considered:

•$Ratio_M$ or Λ should be above a minimum value to guarantee enough distinguishability for the whole cell;

• The programming voltage should not exceed a maximum voltage;

• For memristor, the read speed is much faster than write speed.Therefore, the operation speed mainly depends on the write speed. Thus, the write speed should be lower-bounded;

• Finally, the energy consumption for read and write a memory cell should not exceed certain power budget. Note in this paper, we assume the energy consumption is dominated by the write operation.

Consequently, three different design optimization strategies can be applied for the proposed dual-element memristor-based memory: *energy-driven*, *speed-driven* or R_{ratio}*-driven design* optimization. In this paper, due to the limited space, we focus on the *energy-driven* design optimization to implement a low-power memory cell. However, under other specifications such as high speed or high-distinguishability, the speed-driven or R_{ratio}-driven optimization can be performed as well.

For the energy-driven optimization, the objective is to optimize the programming voltage V_{in} and pulse width t_{pulse} to minimize the write energy consumption E_{write}, given the design requirements of $Ratio_{min}$, Λ_{min}, $Speed_{min}$ and V_{max}. The design space of V_{in} and t_{pulse} for the energy-driven optimization is shown in Fig. 4. Note, the partial programming from low resistant and high resistant side of the memristor consume different amount of energy. Particularly, at the same speed and R_{ratio}, programming from the high resistance side consumes more energy than from the low resistance. Also, the energy consumption increases with the increase of write speed. We should notice that, the upper and lower boundaries of write speed are restricted by the voltage constraints and noise immunity issues, which are denoted as V_{max} and V_{min}. Thus, for a low-power design, we should partially program the low resistance side of the memristor and program at the speed of $Speed_{min}$.

Based on the energy-driven optimization, a low-power dual-element memristor-based memory cell is proposed, which has the same speed and distinguishability as one cell memristor-based memory and consumes considerably less energy.

3.3 Memristor-based memory circuitry design

In this section, a dynamic memristor-based memory is proposed. This design can switch easily between a high-capability mode (normal mode) and a low-capability low-power mode, with very small area and energy overhead compared to general memristor-based memory.

Fig. 5 shows the overall structure of the proposed memory array with peripheral circuits. Generally, the memory struc-

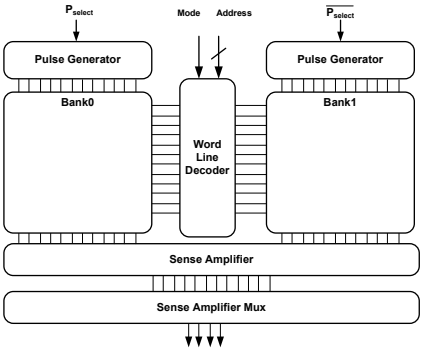


Figure 5: Overall structure of the memory array

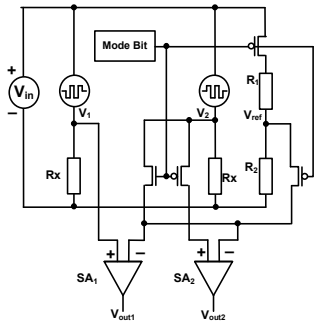


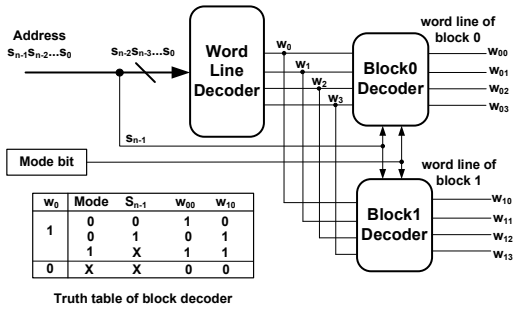
Figure 6: Circuit structure for dual-element memristor-based memory cell

ture is based on the design proposed in [8]. As mentioned, in order to avoid the problems due to the sneak paths, the MOSFET are used as the selector in our design. Moreover, we add several additional circuits to the design, ensuring that the memory can switch between the two modes. The memory is divided into two banks, bank 0 and bank 1. The positive cells are located in bank 0 and the negative cells are located in bank 1. Each bank has its own pulse generator. In Mode 0, two banks work independently, whereas in Mode 1, two banks work together to realize the dual-element memristor-based memory, and each pair of the associated cells are located at the same positions in every bank.

The pulse generator provide different voltage levels to the memory cell. A mode bit is assigned to each pulse generator to choose the voltage level. If mode bit is logic '1', indicating the memory works in low power mode, the low voltage V_L is applied to memristor cells. If mode bit is logic '0', the normal mode uses the high voltage V_H for the circuit.

The read operation is similar to the single-cell memristor memory. As shown in Fig. 3, to extract the information of the cell, a voltage V_{in} is applied across the whole cell and the current is sensed. In Fig. 6, if the mode bit is set to 0, the circuit works as two independent memory cells. The voltage V_1 and V_{ref} are compared in sense amplifier 1 (SA_1). While V_2 and V_{ref} are compared in sense amplifier 2 (SA_2). However, if this bit is set to 1, the circuit works in low-power dual-element mode. The resistors used to generate reference voltage are useless and are isolated. Additionally, the voltage V_1 and V_2 are compared to extract the data.

The modified word line decoder is illustrated in Fig. 7, which contains one traditional decoder and two block decoders. As mentioned, memristors in the dual-element cell locate in the same location of bank 0 and bank 1 respectively. For example, in Fig. 5, the memristors of address "0000" is associated with the memristors at "1000". For each pair of



w0	Mode	Sn-1	w00	w10
1	0	0	1	0
	0	1	0	1
	1	X	1	1
0	X	X	0	0

Figure 7: Word line decoder for dual-element memristor-based memory cell

the associated memristor, only the first bit of the address is different. Thus, to decode the n bit address, a n-1 bit decoder is firstly used to decode the low n-1 bits of the address. After that, two word lines are selected at the same time. Then the highest bit and the mode bit are used together to generate the control signal for the two block decoders, deciding which line or both lines are activated. The truth table for the block decoder is shown in Fig. 7. If the Mode bit is 0, only one line is activated at one time, indicating the memory works at normal mode. Contrarily, if the Mode bit is 1, two word line are activated simultaneously.

4. EXPERIMENTAL RESULTS

4.1 Experiments setup

In our experiments, we model the memristor-based memory structure with 45nm CMOS technology (i.e., the memory storage cells are memristors while the peripheral circuitry are built with 45nm CMOS technology). The Synopsis HSPICE Tool with 45nm technology library is employed to get the delay, energy, and area values of the peripheral circuits of our memory design. Also, we use Cadence Spectre Analog environment to simulate the design of sense amplifier. The memristor parameters and other memory parameters used in the experiments are shown in Table I [8] [11].

Table 1: Experiment Parameters

Parameters	Description	Value
R_{on}/R_{off}	Low/High Resistance	$50/10K\ \Omega$
R_{top}	Resistance of Upper Oxide	$50\ \Omega$
μ_v	Equivalent dopants mobility	$10^{-7}m^2/V \cdot s$
L	Thin Film Thickness	$5nm$
S	Cross section area	$30nm \times 30nm$
N_1/N_2	Memory Size	32MB/16MB
W	World Width	8bits
V_{w0}	Write level voltage at Mode 0	1V
V_{w1}	Write level voltage at Mode 1	1/3V
V_r	Read voltage	1V

4.2 Energy Consumption Optimization

As mentioned in Section 3.2, to design the dual-element memory cell, a trade-off should be made among the energy, speed, and distingushiablility considerations. Three different kinds of designs can be realized by using the dual-element memristor-based memory: energy-driven, speed-driven and R_{ratio}/Λ-driven design. Our experiments mainly focus on the energy-driven optimization. However, we also show some 'intermediate' schemes of the optimization, which demonstrate the speed and distingushiablility improvements of the dual-element cell. For the energy-driven optimization, the problem can be formulated as following:

Table 2: Different Optimization Schemes

Scheme	Resistance	Λ	V_{write}	t_{write}	Energy/Cell
Baseline	$R_l \sim R_h$	0.41V	V_{w0}	25.38ns	3.20pJ
Scheme1	$R_l \sim R_h/2$	0.74V	V_{w1}	19.02ns	3.16pJ
Scheme2	$R_l \sim R_h/3$	0.68V	V_{w1}	8.85ns	2.10pJ
Scheme3	$R_l \sim R_h/4$	0.63V	V_{w1}	4.98ns	1.54pJ
Scheme4	$R_l \sim \sqrt{R_l R_h}$	0.41V	V_{w1}	0.78ns	0.60pJ

Objective: Optimize the programming voltage V_{in}, and pulse width t_{pulse} to minimize write energy E_{write}.

Constrains:

$$\begin{cases} \Lambda > \Lambda_{min} \\ Speed_{write} > Speed_{min} \\ V_{min} < V_{in} < V_{max} \ , \end{cases} \tag{11}$$

According to the energy-driven optimization, four schemes of dual-element memristor-based memory cell are proposed, which are shown in Table. II. *Baseline* is the single-element memristor-based memory, in which the full range of the memristor is used. The other four schemes, scheme 1 to scheme 4, are the proposed dual-element memory with different resistance ranges and write strategies. Especially, Scheme 4 shows the most aggressive optimization of the design, which has the least resistance range and the equivalent distinguishability compared to the baseline scheme. Note that we use Λ and t_{write} as the design constraints in this paper to ensure the dual-element design has the comparable performance to the baseline design. Thus the design constraints are: $\Lambda > \Lambda_{basline} = 0.41V$, $t_{write} < t_{baseline} = 25.38ns$, $V_{max} = 1V$ and $V_{min} = 1/3V$. From this table, we can see that under these constraints, the proposed dual-element memristor-based memory can gain speed, distinguishability and energy improvement with different design schemes. For example, Scheme 1 has the similar energy consumption as the baseline design. However, the distinguishability, denoted as Λ, increases from 0.41V to 0.74V. On the other hand, in the most aggressive scheme (scheme 4), the Λ is equal to $\Lambda_{baseline}$. But the energy consumption is only about 18% of the baseline.

To study the efficiency of the proposed design, we compare the latency and energy consumption for two different memory arrays, which are shown in Fig. 8. It is important to notice that the numbers of memristor used in the same size of memory are different. For example, the baseline design of the 32MB memory has totally $32M \times 8$ memristors. However, the other schemes have $64M \times 8$ memristors. The results show that, although the proposed schemes use doubled number of memristors, the write energy and latency are improved significantly. The energy consumption can be reduced by 40%, and the write latency can be improved by up to 90%.

5. CONCLUSION

In this paper, we perform a comprehensive study to analyze the power and energy consumption of the thin-film memristor. A dual-element memristor-based memory structure is proposed, in which each memory cell contains two memristors that store the complement states. Our proposed design is verified through comprehensive simulation. The experimental results show that under the given design constraints, the proposed dual-element memory can achieve the same programming speed and distinguishability as the baseline single-element memory but the energy consumption can be reduced by up to 80%.

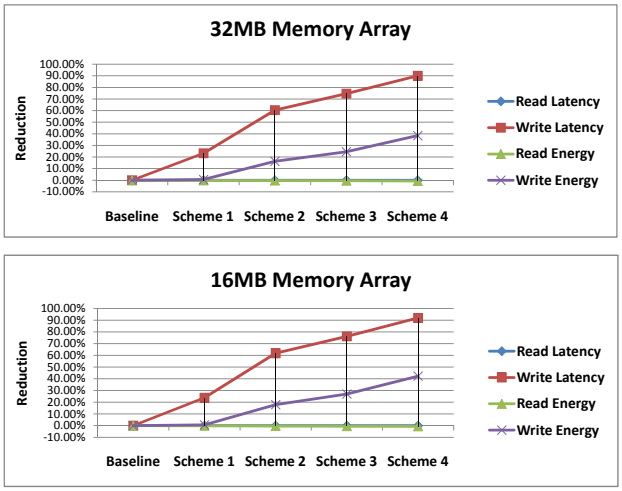


Figure 8: Comparison of latency/energy reduction

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7. REFERENCES

[1] L. Chua. Memristor-the missing circuit element. *IEEE Transactions on Circuit Theory*, (5), Sep 1971.

[2] D. B. Strukov and et al. The missing memristor found. In *Nature*, 2008.

[3] Y. V. Pershin and M. D. Ventra. Experimental demonstration of associative memory with memristive neural networks. In *Nature*, 2009.

[4] H. Choi and et al. An electrically modifiable synapse array of resistive switching memory. *Nanotechnology*, 2009.

[5] Y. V. Pershin and M. D. Ventra. Practical approach to programmable analog circuits with memristors. *Circuits and Systems I: Regular Papers, IEEE Transactions on*, PP(99):1–8, 2010.

[6] Q. Yu and et al. Transmission characteristics study of memristors based op-amp circuits. *ICCCAS*, 2009.

[7] K. Witrisal. A memristor-based multicarrier uwb receiver. *ICUWB*, 2009.

[8] Y Ho, G. M. Huang, and P. Li. Nonvolatile memristor memory: device characteristics and design implications. In *ICCAD*, Nov. 2009.

[9] O. Kavehei and et al. The fourth element: Insights into the memristor. In *ICCCAS*, 2009.

[10] J. M. Tour and T. He. Electronics: The fourth element. In *Nature*, pages 42–43, 2008.

[11] R. Williams. How we found the missing memristor. *IEEE Spectrum*, (12), Dec. 2008.

[12] M. Dong and L. Zhong. Challenges to crossbar integration of nanoscale two-terminal symmetric memory devices. In *NANO*, pages 692 –694, Aug. 2008.

[13] H. Li and Y. Chen. An overview of non-volatile memory technology and the implication for tools and architectures. In *DATE*, 2009.