Impact of Process Variations on Emerging Memristor*

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ABSTRACT

The memristor, known as the fourth basic two-terminal circuit element, has attracted many research interests since the first real device was developed by HP labs in 2008. The nano-scale memristive device has the potential to construct some novel computing systems because of its distinctive characters, such as non-volatility, non-linearity, low-power, and good scalability. These electrical characteristics of memristors are mainly determined by the material characteristic and the fabrication process. For example, process variations may cause the deviation of the actual electrical behavior of memristors from the original design and result in the malfunction of the device. Therefore, it is very important to understand and characterize the impact of process variations on the electrical behaviors of the memristor and its implication to the circuit design. In this paper, we analyze the impact of the geometry variations on the electrical characteristics of the memristor. Two parameters - NARD (Normalized Accumulative Resistance Deviation) and NAARD (Normalized Accumulative Absolute Resistance Deviation), are introduced to measure the fluctuation of the overall internal state (or the resistance) of a memristor under the impact of process variations. Based on our analysis, Monte-Carlo simulations are conducted to evaluate the device mismatch effects in the memristor-based memory.

Categories and Subject Descriptors

B.4 [**Performance and reliability**]: Performance Analysis and Design Aids.

General Terms

Measurement, Performance, Reliability.

Keywords

Memristor, process variation, nonvolatile memory.

1. INTRODUCTION

The memristor, known as the fourth basic circuit element, was first theoretically predicted by Chua in 1971 [1], and practically demonstrated by HP Labs in 2008 [2]. This emerging technology has many distinctive features, including non-volatility, non-linearity, low-power, and good scalability. Such properties provide memristor the potential to implement novel forms of computing. For example, the properties of non-volatility and scalability make the memristor a promising candidate as the next-generation high-density, high-performance memory technology [3]. Moreover, as the memristor can accomplish most of the behaviors of the synapse such as remembering the past dynamic history and storing a continuous set of states, it has the potential to realize electronic neural networks [4] [5]. Also, some practical approaches of programmable analog circuits with memristor have been proposed [6].

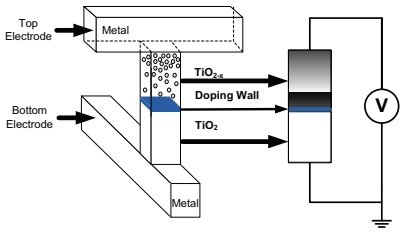

Figure 1: Structure of memristor cell.

As the process technology scales, device parameter fluctuations induced by process variations such as line-edge roughnesses (LERs), oxide thickness fluctuations (OTFs), and random discrete dopants (RDDs) have become critical issues in affecting the performance of devices [7]. Among these variations, LER is one of the random variations caused by random uncertainties in the process of lithograph and etching. It results in a random deviation of line edge print-images from its ideal pattern [8]. Since LER does not decrease as the device shrinks due to fundamental problems with the molecular structure of the photoresist, it is reported as the key variation problem of device fluctuations in sub-45nm designs [9]. Because the memristor is implemented on the basis of the thin-film deposition technology, it is important to evaluate the impact of the process variations on the electrical behavior of the memristor.

In this paper, for the first time, we perform a comprehensive study to analyze the impact of three-dimension (3D) process variations on the physical characteristic of the memristor. The NARD (normalized accumulative resistance deviation) and NAARD (normalized accumulative absolute resistance deviation) are proposed as the parameters to evaluate the overall internal state (or the resistance) fluctuation under the effect of process variations. Based on the mathematical analysis, Monte-Carlo simulation is applied to examine the device mismatch effects of the memristor based memory.

2. PRELIMINARIES

Fig. 1 shows a conceptual view of memristor structure from HP Labs [2]. The top electrode and bottom electrode are two metal nanowires on *Pt*, and the thin titanium dioxide film is sandwiched by the electrodes. Shortly after the demonstration of HP's memristor, researches have begun to look for other possible memristors. The memristor using CMOS-compatible process was proposed recently [10], and it has the similar structure of HP's memristor but the p-doped silicon is used as the bottom electrode. With this process, the memristor can be fabricated directly on a silicon substrate. In addition, a new spintronic memristor is demonstrated based upon spin-torque-induced magnetization switching and magnetic-domain-wall motion [11].

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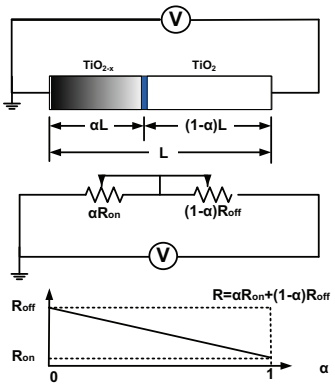

Figure 2: Circuit model of memristor [2].

2.1 Memristor and mathematical model

The memristor is formally defined as a two-terminal element in which the magnetic flux between the terminals is a function of the amount of electric charge q that can pass through the device, which is explicitly expressed by the equation $d\varphi = Mdq$. Since the magnetic flux is the integration of the voltage, and the charge is the integration of the current, the memristance has the same unit as the resistance. Considering that the memristance is a function of charge, the definition of memristor can be generalized as:

$$\begin{cases} V = M(\omega)I \\ d\omega/dt = f(\omega, i) \ , \end{cases}$$

where ω is the state variable, depending on the integral of current profile over time.

In this paper, we study the $Pt/TiO_2/Pt$ memristor of HP Labs [2], which is shown in Fig. 1. The 50-nm-wide TiO_2 thin film is sandwiched by two metal wires. The stoichiometric TiO_2, whose ratio of oxygen to titanium is exactly 2 to 1, has its natural state as an insulator. On the other hand, if the titanium dioxide is lack of a small amount of oxygen, its conductivity becomes relatively high as a semiconductor and it is called oxygen-deficient titanium dioxide. A biased voltage, which is applied across the thin film, will drive the oxygen vacancies into the pure TiO_2 and therefore lower the resistance continuously. A reversed bias voltage will push the dopants back to its position and raise the resistance.

A coupled variable resistor model for this memristor is shown in Fig. 2. The total thickness of the TiO_2 thin film is denoted as L, and the overall resistance is determined by two resistors connected in series. The internal state of the memristor, denoted as α ($0 \leq \alpha \leq 1$), is defined as the proportion between the length of doped region and the total length. If the memristor is fully undoped, it has very high resistance, denoted as R_{off}. Likewise, the resistance of fully doped memristor is low, and is denoted as R_{on}. Thus, the overall resistance of the memristor cell is:

$$R(\alpha) = \alpha R_{on} + (1-\alpha)R_{off} \ . \tag{1}$$

When a biased voltage $v(t)$ is applied across the memristor, the length of the doping region will change. For example, a positive voltage ($v(t) > 0$) will cause the dopants (oxygen vacancies) drifting to the undoped region and therefore will result in a lower resistance of the whole memristor. On the opposite side, a negative biased voltage ($v(t) < 0$) will shrink the doped region and will increase the resistance. The behavior can be summarized as follow [2]:

$$\begin{cases} v(t) = (\alpha R_{on} + (1-\alpha)R_{off}) \cdot i(t) \\ \frac{d\alpha}{dt} = \mu_v \frac{R_{on}}{L^2} i(t) \ , \end{cases} \tag{2}$$

where $v(t)$ is the voltage applied across the memristor, $i(t)$ is the current through it and μ_v is the equivalent mobility of dopants. By solving the differential equation, and applying the initial

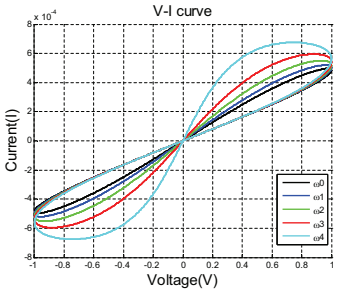

Figure 3: I-V Curve of different input frequency (φ).

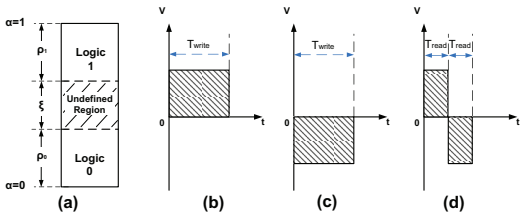

Figure 4: Write/Read operation of memristor based memory cell.

condition ($\alpha(0) = \alpha_0, \varphi(0) = 0$), we can get the relation between the state $\alpha(t)$ and the flux $\varphi(t)$ as:

$$\alpha(t) = \gamma - \sqrt{(\alpha_0 - \gamma)^2 - \frac{2\mu_v}{L^2}(\gamma - 1)\varphi(t)} \ , \tag{3}$$

where $\gamma = R_{off}/(R_{off} - R_{on})$. From the definition of α, the constraint $0 \leq \alpha \leq 1$ requires a corresponding constraint to the flux $\varphi(t)$:

$$\frac{(\gamma - \alpha_0)^2 - \gamma^2}{r-1} \cdot \frac{L^2}{2\mu_v} \leq \varphi(t) \leq \frac{(\gamma - \alpha_0)^2 - (\gamma-1)^2}{r-1} \cdot \frac{L^2}{2\mu_v} \ . \tag{4}$$

If a sinusoidal voltage is applied to the cell and the flux applied to the cell meet the constraint in Equation (4), the internal state α continually increases from the initial state α_0 as long as the voltage is positive, and it means the input flux φ is greater than 0. On the other hand, if the input voltage is negative, the state α decreases from a high value to a low value. If only the net input flux is equal to zero, the state comes back to initial state α_0. The Voltage-Current characteristics of the memristor is shown in Fig. 3. Since the net input flux varies with the frequency of the input voltage, the I-V curve also varies with the frequency of the input voltage.

2.2 Memristor based Memory

The distinct properties of the memristor such as nonvolatility, low-power, and scalability make it a promising candidate as the next-generation high-density, and high-performance memory technology [2] [3]. In the presence of noises, a safety margin should be defined to ensure the reliability of the cells. The safety region and the undefined region for a memristor cell is shown in Fig. 4(a). The internal state $0 < \alpha < \rho$ represents logic '0'; $(1-\rho) < \alpha < 1$ represents logic '1'; and $\rho < \alpha < (1-\rho)$ represents the undefined margin.

The structure of memristor-based memory proposed in Ho's work [3] is shown in Fig. 5. The main structure of the memristor-based memory is similar to the typical memory, including the row decoder, the column decoder, and the sense amplifier. The most important operations to the memristor-based memory are the write operation (including write logic '1' and logic '0'), the read operation, and the refreshing operation.

1. The **write operation** is to apply sufficient flux to the memristor cell and therefore write logic '1' (apply positive flux) or logic '0' (apply negative flux). A simple way to obtain enough flux is to apply a square wave pulse to the cell, which is shown in Fig. 4 (b) (c). The magnitude of input voltage is denoted as V_{in}. Also, the safety region for

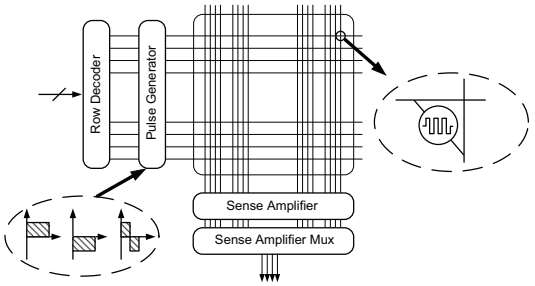

Figure 5: Structure of memristor based memory.

logic '1', logic '0', and undefined region are ρ_1, ρ_0, and ξ. To ensure the cell is written to an ideal state, the pulse width should be larger than a time restriction:

$$T_{write} \geq \eta_w \frac{L^2}{2\mu_v V_{in}} \ , \tag{5}$$

where

$$\eta_w = max(\ \frac{\gamma^2 - (\gamma - 1 + \rho_1)^2}{r-1} \ , \ \frac{(\gamma - \rho_0)^2 - (\gamma - 1)^2}{r-1} \ ) \ . \tag{6}$$

2. The **read operation** is more complicated. As mentioned, if the net input flux is not equal to zero, the doping wall will move to the direction corresponding to the direction of flux. Therefore, the internal state will be sensitive to the read operation. In order to ensure stabilization of the memristor internal state, a two-stage read operation is proposed [3], which is shown in Fig. 4 (d). The ideal read pattern is a negative pulse and a positive pulse with the same magnitude(V_{in}) and duration (T_{read}), importing zero net flux into the memristor cell.

   Considering the scenario that the initial state is $\alpha_0 = 0$ and a negative voltage pulse is first applied to the memristor cell, it will not disturb the internal state, but the following positive pulse will lead the internal state away from original state. If the internal state moves beyond the safety region, an error may occur during the next read operation. Thus, the read pulse width should have a constraint associated with the safety margin, described as:

$$T_{read} \leq \frac{L^2}{2\mu_v V_{in}} \frac{3\gamma\alpha_{Tolerance} - \alpha^2_{Tolerance}}{\gamma - 1} \ , \tag{7}$$

   where the tolerance level parameter $\alpha_{Tolerance}$ is the maximum value of internal state disturbance in this scenario and satisfies $\alpha_{Tolerance\ i} < \rho_i$, $i = 0, 1$.

3. The ideal read operation provides zero net flux to the memristor cell and requires the negative and the positive pulses to have exactly the same duration. But if the width mismatch exists, the net flux becomes nonzero. After several read operations, the accumulative net flux will disturb the internal state and result in soft errors. Thus, given a boundary of the difference between negative and positive pulse widths, a **refreshing operation** is needed to refresh the internal state for every $N_{refresh}$ read operation.

3. STATISTICAL ANALYSIS

In this section, we first describe the property of our statistical analysis for the impact of process variations on memristor resistance. We then define the NARD and NAARD as parameters to evaluate the impact under the linear case and the non-linear case, respectively. The mathematical simulation shows that the NARD and NAARD can represent the overall deviation of the internal state and the resistance of the memristor from the original parameters.

3.1 Memristor model under process variations

The process variations exist in three-dimension of the thin film memristor, and arise from lithographic patterning methods and deposition processes, respectively. Two of these variations result in the cross section area variation, and the other one leads to the variation of the thickness. Therefore, we have to distinguish the different impacts on the memristor brought by these two types of process variations.

The memristor model under the process variations is derived from Equation (1), where the resistance of a memristor can be expressed as the linear combination of the doped resistance (R_{on}) and the undoped resistance (R_{off}). Note that the definition of the resistance in Equation (1) is under the assumptions that the cross section and the thickness of the thin film are constant. Therefore, considering the variation of the cross section, the general resistance model of the memristor should be calculated as:

$$R(\alpha, \ L, \ S) = \int_0^{\alpha L} \frac{\rho_{on}}{S(\alpha)} dl + \int_{\alpha L}^{L} \frac{\rho_{off}}{S(\alpha)} dl \ , \tag{8}$$

where ρ_{on} and ρ_{off} are the electrical resistivities of the doped and the undoped TiO_2 thin film, the L is the device thickness, and the $S(l)$ is the cross-sectional area varying with the location in the direction of device thickness. Therefore, the V-I relation of the memristor can be derived as:

$$\begin{cases} V(t) = (\int_0^{\alpha L} \frac{\rho_{on}}{S(\alpha)} dl + \int_{\alpha L}^{L} \frac{\rho_{off}}{S(\alpha)} dl) i(t) \\ d\alpha/dt = \mu_v \frac{\rho_{on}}{L \cdot S(\alpha)} i(t) \ . \end{cases} \tag{9}$$

3.2 Impact of process variations on memristor

Cross Section Area. As aforementioned, the variation of area along with the device thickness direction is extremely small and negligible. Therefore, we can consider the cross section area as a constant S'. Then Equation (1) becomes:

$$\begin{aligned} R'(\alpha, \ L, \ S) &= \int_0^{\alpha L} \frac{\rho_{on}}{S'} dl + \int_{\alpha L}^{L} \frac{\rho_{off}}{S'} dl \\ &= \frac{S}{S'} \times [\alpha R_{on} + (1 - \alpha) R_{off}] \ . \end{aligned} \tag{10}$$

Note, the left part of the last expression is exactly the ideal resistance of the memristor. Therefore, the resistance under process variations can be calculated by multiplying the ideal resistance by a factor θ. To facilitate out discussion, we defined: $\theta_{Area} = S'/S$. Thus we get:

$$R'(\alpha, \ L, \ S) = \frac{1}{\theta_{Area}} R(\alpha) \ . \tag{11}$$

In order to illustrate how the process variations affect the physical characteristics of memristor, we apply different degrees of variation to the cross section area. The relationship between net input flux (φ) and the resistance is shown in Fig. 6. One can observe that the negative variation of cross section area will increase memristor's resistance when the same flux is applied. On the contrary, positive variation leads to the decrease of the resistance.

Thickness. Process variations also exist on the thickness of the thin film material. Although the thickness variation is not as much as the cross section area variation, it is still a factor influencing the physical characteristics of the memristor. If we only consider the thickness variation first, Equation (1) can be recalculated as:

$$\begin{aligned} R'(\alpha, \ L, \ S) &= \int_0^{\alpha L'} \frac{\rho_{on}}{S} dl + \int_{\alpha L'}^{L'} \frac{\rho_{off}}{S} dl \\ &= \frac{L'}{L} \times [\alpha R_{on} + (1 - \alpha) R_{off}] \ , \end{aligned} \tag{12}$$

which is similar to Equation (10). Therefore the resistance is still a linear combination of R_{on} and R_{off}, and is in proportion

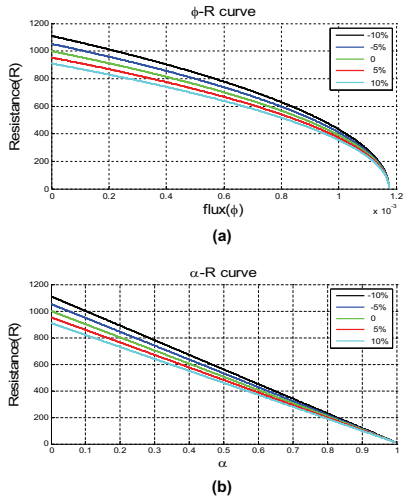

Figure 6: Impact of cross section area variation.

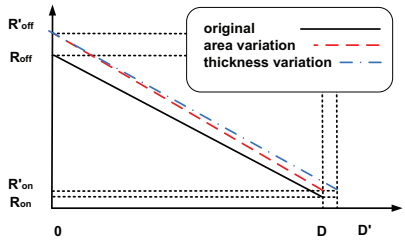

Figure 7: Resistance under the area and thickness variation.

to L'/L. We define the proportion as $\theta_{Thick} = L'/L$, then

$$R'(\alpha,\ L,\ S) = \theta_{Thick} R(\alpha) \quad . \tag{13}$$

The expressions of resistance in Equation (11) and Equation (13) are similar to each other. Thus the ϕ-R curve and α-R curve are very similar to Fig. 6. In addition, we can easily conclude that these two equations will be equivalent when $\theta_{Area}\theta_{Thick} = 1$ is satisfied. However, it is important to be aware of the following facts:

a) Based on the definition of the parameter θ_{Area} and θ_{Thick}, process variations on the cross section area and on the thickness affect the resistance in opposite ways. Large cross section area results in the reduction of resistance and large thickness leads to the increase of resistance.

b) Note, we only consider the relation between the resistance and the internal state α. However, similar α-resistance relation does not imply the same location (l)-resistance relation. As shown in Fig. 7, the broken line and the dash-dot line represent the resistance under the area variation and thickness variation, respectively, with the parameters satisfying the relation $\theta_{Area}\theta_{Thick} = 1$.

c) Based upon the fact that both internal state parameter α and location l can represent the transient state and the resistance of memristor, we can use either of them as the indicator of the memristor state. Considering the uniformity, the normalized parameter α is applied as a standard parameter to evaluate the impact of process variations, which is detailed in Section 3.3.

3.3 Normalized Accumulative Resistance Deviation

In this section, we propose a criterion to evaluate the strength of the effect of process variations on the memristor. In order to represent the overall deviation of memristor characteristics, we should find a general parameter that neither scales with the device size nor changes with the voltage or current input to the cell, and is monotonic to the degree of the process variations. As

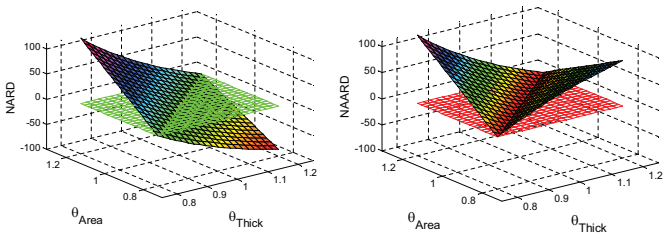

Figure 8: NARD and NAARD as function of process variations.

mentioned, the NARD and NAARD are proposed to evaluate the strength of process variations. The general definition of NARD is:

$$\mathbf{NARD} = \int_0^1 \frac{\Delta R(\alpha)}{R_{on}} d\alpha \ , \tag{14}$$

where

$$\begin{aligned} \Delta R(\alpha) &= \hat{R}(\alpha) - R_0(\alpha) \\ &= \rho_{on} \int_0^{\alpha L} (\frac{1}{S(l)} - \frac{1}{S}) dl + \rho_{off} \int_{\alpha L}^{L} (\frac{1}{S(l)} - \frac{1}{S}) dl \quad . \end{aligned} \tag{15}$$

This definition is applicable to arbitrary memristor model and can represent the degree of memristor's physical characteristic deviation. Particularly, if we consider the variation models discussed in this paper and substitute Equation (11) and Equation (13) into Equation (15), we get:

$$\mathbf{NARD} = \int_0^1 \frac{\Delta R(\alpha)}{R_{on}} d\alpha = \frac{1}{\gamma - 1} (\frac{\theta_{Area}}{\theta_{Thick}} - 1) \ .$$

Notice that the NARD is a signed parameter and can appropriately represent the deviation of the resistance deviation for our linear model. However, for the general model expressed in Equation (8), if the cross section area is no longer a constant and can vary with the thickness direction, the opposite resistance difference may offset each other's contribution to Equation (14). Therefore, we also define another unsigned parameter, NAARD, for the non-linear variation case:

$$\mathbf{NAARD} = \int_0^1 |\frac{\Delta R(\alpha)}{R_{on}}| d\alpha \ . \tag{16}$$

NARD and NARD values under different variation θ_{Area} and θ_{Thick} are shown in Fig. 8. NARD equals to 0 when $\theta_{Area}\theta_{Thick} = 1$. Otherwise, the NARD increases (decrease) with the increase (decrease) of θ_{Thick} or the decrease (increase) of θ_{Area}. As mentioned earlier, NAARD is the absolute value of NARD under the linear model. Although it can also reflect the degree of impacts of process variations, it does not contain any information of the direction. Thus, the NARD is more suitable for linear model.

4. EXPERIMENTAL RESULTS

4.1 Experiments setup

The LER and the consequent line-width roughness (LWR) have been comprehensivly studied [8] [12]. The process variations in the cross section area are introduced due to the lithographic patterning method, and are similar to LER and LWR. As shown in Fig. 9, the LER exists in all of the four edges of the cross section. Thus, we should model the LER for each edge and evaluate the area variations resulting from the LER. In this paper, the LER is generated via a Gaussian autocorrelation function [7] [13]. The algorithm to generate the LER is shown in Fig. 10. This algorithm starts from a power spectrum for Gaussian autocorrelation function, which is denoted as

$$P_{Gaussian}(k) = \sqrt{\pi}\Delta^2 \Lambda e^{-k^2\Lambda^2/4} \ . \tag{17}$$

The parameter Δ is the RMS amplitude and Λ is the correlation length. Δ is the standard deviation of the line edge and the LER is traditionally defined as 3Δ. In our simulation, we

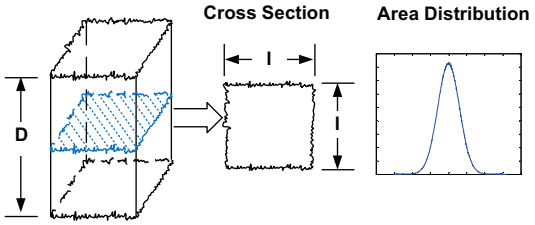

Figure 9: Cross section area variation.

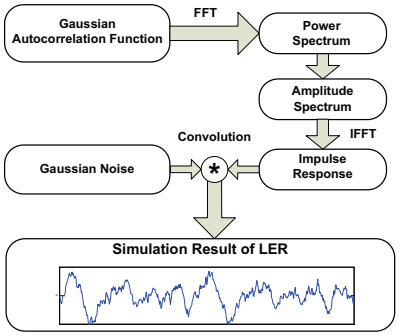

Figure 10: Process to simulate LER.

first choose the typical value of the LER parameters reported in [7] ($\Delta = 2nm$, and $\Lambda = 20nm$). Then we scale down these parameters to evaluate the impacts under different degrees of process variations.

After a square root operation, the amplitude of the power spectrum is transformed to the impulse response by an inverse Fourier transformation. Finally, the resulting impulse response function is convolved with a Gaussian noise to generate the desired random line edge samples.

The thickness variation is caused by the random uncertainties in the process of sputter deposition or atomic layer deposition. Thus, the LER model is not suitable for thickness variation. Considering the thickness variation is much smaller than that of cross section, in this paper, we assume that the thickness variation has a gaussian distribution with $\mu = 0$ and $\sigma = 1\% \times Thickness$. By using these model, the Monte-Carlo simulation is used to evaluate the impact of process variations on the memristor based memory, which is mentioned in Section 2.2.

Other parameters used in our Monte-Carlo simulation are shown in Table. 1.

4.2 Memristor based memory

4.2.1 NARD/NAARD distribution

As mentioned in Section 3.3, NARD and NAARD can represent the over resistance deviation of a memristor under process variations. Therefore, under the impact of process variations, NARDs and NAARDs also spread from a fixed value to a statistical distribution. The typical distributions of NARD and NAARD are shown in Fig. 11. If we reduce the Δ from 2nm to 1nm and 0.5nm, the impact of process variations will decrease,

Table 1: Simulation Parameters

Parameters	Description	Value
R_{on} / R_{off}	Low/High Resistance	$10/1000\Omega$
γ	$R_{off}/(R_{on} - R_{off})$	100/99
μ_v	Equivalent dopants mobility	$10^{-6}m^2/V \cdot s$
L	Thin Film Thickness	$5nm$
S	Cross section area	$30nm \times 30nm$
Δ_{area}	RMS amplitude of LER in cross section	$2nm$(typical) / $1nm$ / $0.5nm$
Λ_{area}	Correlation length of LER in cross section	$20nm$(typical) / $10nm$ / $5nm$
σ_{thick}	STD of thin film thickness	$0.3nm$
ρ_0 ρ_1	Safety margin for logic '0'/ '1'	0.4/0.4
V_w / V_r	Magnitude of write/read square pulse wave	$1V/0.1V$
N	Sample size	100000

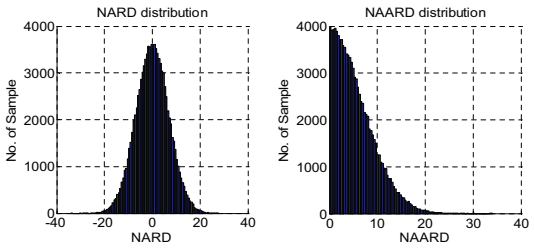

Figure 11: Distribution of NARD and NAARD.

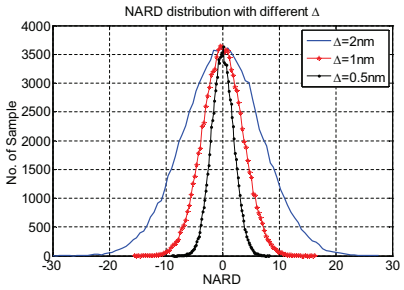

Figure 12: NARD distribution with different Δ.

resulting in the convergence of the NARD distribution, which is shown in Fig. 12. In this figure, we can see the STD of the NARD distribution decreases as Δ decreases, which means the memristor has better resilience to process variations.

4.2.2 Safety Margin

In order to read the internal state of a memristor based memory cell, a read voltage is applied to the memristor cell, and the current through the cell can represent the state information. Therefore, the safety margin for a memory cell depends on the resistance of the cell. Since process variations impact both the internal state and the resistance of a memristor, they also degrade the safety margin of a memristor-based memory cell. As shown in Fig. 4(a), we assume the parameters have the values: $\rho_0 = \rho_1 = 0.4$, which means the undefined margin ξ equals to 0.2. To evaluate the safety margin deviation, we apply the same voltage (or flux) to the cell and calculate the actual resistance of the cell. Then the resistance is in proportion to the current and can reflect the result of read operation.

As shown in Fig. 13, under the process variations, the actual resistance after a write operation (from logic '0' to '1' or from logic '1' to '0') is no longer a fixed value, but spreads into a statistical distribution. In this case, some of the data spreads into the undefined region, and can not be identified by the read circuits, resulting in the loss of data. In order to resolve this problem, we can either enlarge the safety region or reduce the tolerance level by increasing the net flux injecting to the cell. In the ideal situation, the tolerance level can be the same value as the safety region. Therefore, in our simulation, the ideal value of tolerance level is 0.4. If we retain the same tolerance value as 0.4, we have to enlarge the safety region to ensure more samples will be read correctly. As shown in Fig. 13, if we still want to keep 95% samples in the safety margin, the safety margins for logic '0' and logic '1' have to increase from 0.4 to 0.46 and from 0.4 to 0.45, respectively. However, the drawback of this method is the undefined region shrink from 0.2 to 0.08, lead to a decrease of the noise immunity. In addition, with the increase of process variations, the safety region of logic '1' and '0' will become much closer to each other, or even overlap with each other. In this case, we have to reduce the tolerance level to provide a better distinguishbility for the cell. Table. 2 shows the desired values of $\alpha_{Tolerance0}$ and $\alpha_{Tolerance1}$, which can promise 95% samples enclosed by the region $0 < \alpha < 0.4$ and $0.6 < \alpha < 1$.

4.2.3 Write Operation

As shown in Table. 2, in order to guarantee the reliability of memristor cell, the value of the tolerance level should decrease.

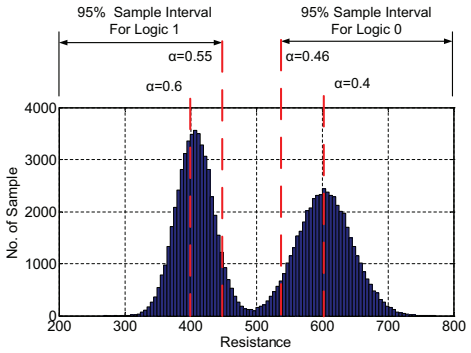

Figure 13: Safety margin variation.

Table 2: Upper bound of $\alpha_{Tolerance0}$ / $\alpha_{Tolerance1}$ under process variations

	$\Lambda = 20nm$	$\Lambda = 10nm$	$\Lambda = 5nm$
$\Delta = 2nm$	0.322 / 0.358	0.334 / 0.364	0.348 / 0.370
$\Delta = 1nm$	0.364 / 0.378	0.368 / 0.382	0.374 / 0.384
$\Delta = 0.5nm$	0.380 / 0.388	0.382 / 0.390	0.386 / 0.392

In this case, we have to apply more flux to write the memristor cell. Therefore, we have to either increase the voltage magnitude or increase the pulse width to provide more flux. In our study, the input voltage is a square wave with the magnitude of V_{in}. Note that the energy consumption is proportional to the latency and to the square of the voltage. Thus, considering the energy issue, it is reasonable to increase the write pulse width to generate more flux. Since the write time becomes larger, the write speed is reduced. Table. 3 shows the write pulse width requirements and the speed degradation under process variations. Fig. 14 shows the energy consumption for writing a memristor with different process variations. One can observe that in the worse case of $\Delta = 2nm$ and $\Lambda = 20nm$, the write energy consumption increases by about 10%.

4.2.4 *Refreshing Scheme*

Another important issue for the memristor based memory is the refreshing scheme. If the read operation can not provide zero flux input, the internal state of memristor may 'drift' to one direction continuously due to the accumulative effect of the input flux [3]. Therefore, after a particular number of reading operations, a refresh operation is needed to eliminate the effect of read pulse mismatch. Normally, we can estimate a upper bound of the pulse mismatch ε_{read}, defined as $\Delta T = \varepsilon_{read} \times T$. Then a refreshing cycle number $N_{refresh}$ can be extracted. We assume $\varepsilon_{read} = 10\%$, and the read pulse width is 0.1ns. The tolerance level are $\alpha_{Tolerance} = 0.2$ and $\alpha_{Tolerance} = 0.1$. Also, for the sake of brevity, we only consider the case of $\Lambda = 20nm$. Then the refreshing schemes under different pulse mismatch bounds are shown in Table. 4. Take $\alpha_{Tolerance} = 0.2$ as an example, the number of refreshing cycles is reduced from 60 to 38 in the worse case, resulting an extra 58% refreshing overhead.

5. CONCLUSION

As technology scales, process variations have become one of the most critical design challenges in nanometer circuit design, resulting in more significant deviation from the nominal value of device parameters. In this paper, we analyzed the impact of three-dimension (3D) process variations on the memristor. The normalized parameters–NARD and NAARD are proposed to describe the overall deviation of the physical characters of memristor under the presence of process variations. It is the first proposal of a general parameter which can be used to evaluates the deviation of the memristor's physical characteristics.

The experimental results show that the process variations reduce safety margin of the memristor by 10%, and extra energy is required to eliminate the impact of process variations. Simulation results indicate the energy consumption for writing a memristor cell increases by up to 10%. Also, the number of refreshing cycles will be reduced by up to 58%, resulting in an extra refreshing overhead to the memristor based memory.

Table 3: Write pulse width requirement

		$\Lambda =$	20nm	10nm	5nm
$\Delta = 2nm$	T_{write}		1.128ns	1.119ns	1.107ns
	Speed degradation		6.5%	5.9%	4.8%
$\Delta = 1nm$	T_{write}		1.093ns	1.088ns	1.084ns
	Speed degradation		3.5%	3.0%	2.7%
$\Delta = 0.5nm$	T_{write}		1.076ns	1.074	1.072
	Speed degradation		2.0%	1.8%	1.7%

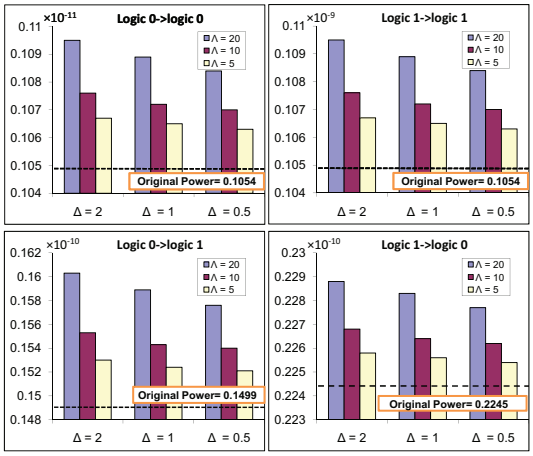

Figure 14: Write energy variations.

Table 4: Refreshing Scheme

	$\alpha_{Tolerance} = 0.1$	$\alpha_{Tolerance} = 0.2$
Δ	$N_{refresh}$	$N_{refresh}$
0	70	60
$0.5nm$	68	55
$1nm$	66	50
$2nm$	61	38

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