Gushu Li

Ph.D Student, University of California at Santa Barbara (UCSB)
gushuli@ece.ucsb.edu
https://sites.google.com/view/gushuli
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Education

2017 - now **University of California, Santa Barbara** **Santa Barbara, CA, US**
Ph.D. Student in Electrical and Computer Engineering
Advisor: Yuan Xie

2015 - 2017 **University of Chicago** **Chicago, IL, US**
Ph.D. Student in Computer Science

2011 - 2015 **Tsinghua University** **Beijing, P.R.China**
B.E. in Electronic Engineering
Thesis: *GPU Hybrid Register File Design*

Work Experience

2018.7 - 2018.9 **Alibaba Group, U.S., Inc.** **Sunnyvale, CA, US**
DAMO Academy - Research Intern
Research Topic: Architecture Specific Quantum Computing Compiler Backend Optimization
Work withr: Yuan Xie, Weifeng Zhang

Publications

[1] **Gushu Li**, Yufei Ding, and Yuan Xie "Tackling the Qubit Mapping Problem for NISQ-Era Quantum Devices" To appear in **ASPLOS** 2019, arxiv preprint 1809.02573

[2] **Gushu Li**, Guohao Dai, Shuangchen Li, Yu Wang, and Yuan Xie "GraphIA: An In-situ Accelerator for Large-scale Graph Processing" International Symposium on Memory Systems (**MEMSYS**), 2018

[3] **Gushu Li**, Xiaoming Chen, Guangyu Sun, Henry Hoffmann, Yongpan Liu, Yu Wang, and Huazhong Yang "A STT-RAM-based Low-Power Hybrid Register File for GPGPUs" Proc. *ACM/IEEE Design Automation Conference (**DAC**)*, 2015.

[4] Haixiao Du, Xuhong Liao, Mingrui Xia, Qixiang Lin, **Gushu Li**, Yuze Chi, Huazhong Yang, Yu Wang, Yong He "Test-Retest Reliability of Graph Metrics in High-Resolution Functional Connectomics: A Resting-State Functional MRI Study" *CNS Neuroscience & Therapeutics (**CNSNT**)*, vol.21, No.10, 2015, pp.802-816.

Awards and Honors

2017 **Regents Fellowship**, Electrical and Computer Engineering, UCSB
2017 **International Doctoral Recruitment Fellowship**, UCSB
2016 **Student Travel Grants**, IEEE VLSI Test Symposium
2016 **University Unrestricted Fellowship**, University of Chicago
2015 **A. Richard Newton Young Student Fellow Scholarship**, Design Automation Conference
2014 **Scholarship for Academic Excellence**, Tsinghua Unviersity
2012 **Scholarship for Academic Excellence**, Tsinghua Unviersity

Research Summary

Gushu Li has been a researcher across computer architecture, quantum computing, parallel programming, and emerging non-volatile memory regions. His recent research interests include (1) Quantum Computer Architecture, (2) Processing-in-memory and in-situ Architecture, (3) GPU architecture. The research projects are listed as follows,

Architectural Support for Quantum Computing *(Quantum Computing, 2017 - **present**)*

Many important problems can not be efficiently solved on classical computers while quantum computing brings us a new opportunity to solve some of the hard problems in polynomial time. As there have been significant achievements in quantum computing area in the last few decades, intermediate-scale quantum devices are becoming available. In the noisy intermediate-scale quantum (NISQ) era, more and more hardware constraints appear and can be addressed from architecture level. In this

project, we will look into emerging quantum devices, abstract architectural level constraints, and then try to optimize the entire quantum computing system.

Processing-in-Memory and in-situ Architectures *(Computer Architecture, 2017 - **present**)*

As technology scales, data movement is becoming the bottleneck of today's von Neumann architecture based computing system which separates the processing units and memory units. Processing-in-memory (PIM) and in-situ accelerators are promising approaches to close this gap between computing and memory. We can significantly improve latency, bandwidth, and power by moving computation closer to the memory. In this project, we will explore novel PIM and in-situ architectures for memory intensive applications.

Low-Power GPU Register File Design *(Computer Architecture, 2014-2015)*

GPUs have been widely used to accelerate various applications. Previous results show that 20% to 40% of GPU power is consumed by the large SRAM-based register file due to its high leakage power. Non-volatile memory (NVM) is a potential replacement for SRAM. To overcome performance degradation caused by the long write latency of NVM, we proposed a hybrid register file and mixed SRAM-based write buffers with a warp-aware write back strategy. Our design leveraged the intrinsic feature of a GPU register file to hide the long write time of NVM during context switch.

- *DAC'15.*

Parallel Program Design on GPU *(Parallel Programming, 2012-2014)*

We developed a GPU version of an edge-based graph partition algorithm, which was 10 times faster than the corresponding well-optimized CPU version. This project achieved top 10 in AMD Heterogeneous Computing Competition in China.
We also implemented a probabilistic fiber tractography algorithm on GPU. In this project, I introduced variable step size in the iteration to solve the thread load balance problem and reduce the communication overhead between CPU and GPU with 40 times acceleration. This algorithm was integrated into a brain network analysis platform.

- *Top 10 in AMD APU/GPU Heterogeneous Computing Competition 2012 in China*
- *CNSNT'15*

Teaching Experience

2015 Fall	TA for Advanced Programming, MPCS 51100, Prof. Andrew Siegel
2016 Winter	TA for Computer Architecture, MPCS 52010, Prof. Todd Nugent
2016 Fall	TA for Computer Architecture, CMSC 22200, Prof. Yanjing Li
2017 Winter	TA for Mobile Computing, CMSC 23400, Prof. Andrew Chien
2017 Spring	TA for Usable Security and Privacy, CMSC 23210, Prof. Blase Ur

Technical Skills

Programming Language	C/C++, Python, Matlab, CUDA, OpenCL, Verilog
Tools	GPGPU-SIM, GEM5